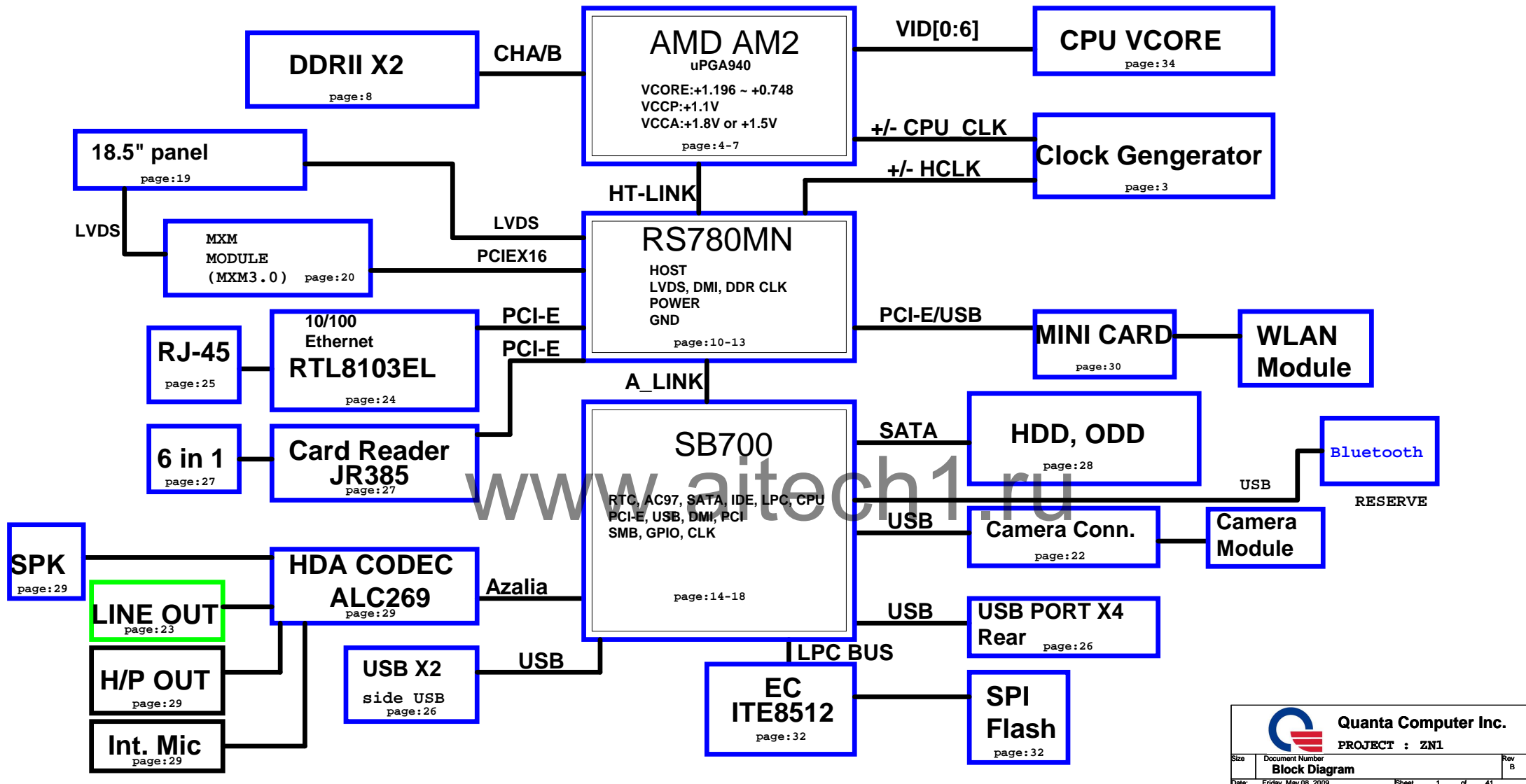


Amazon LCD PC Block Diagram

1

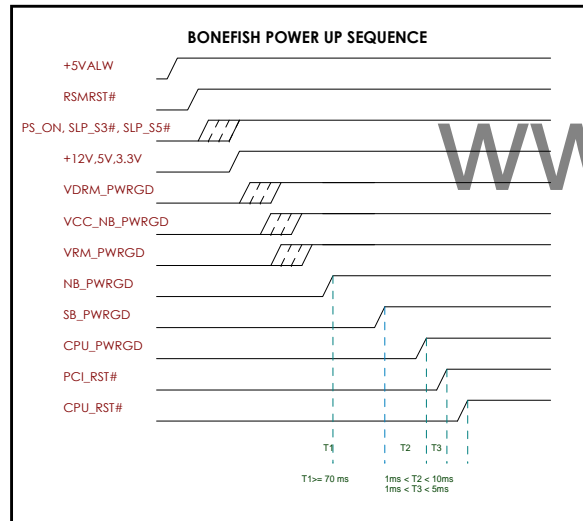


PCB STACK UP

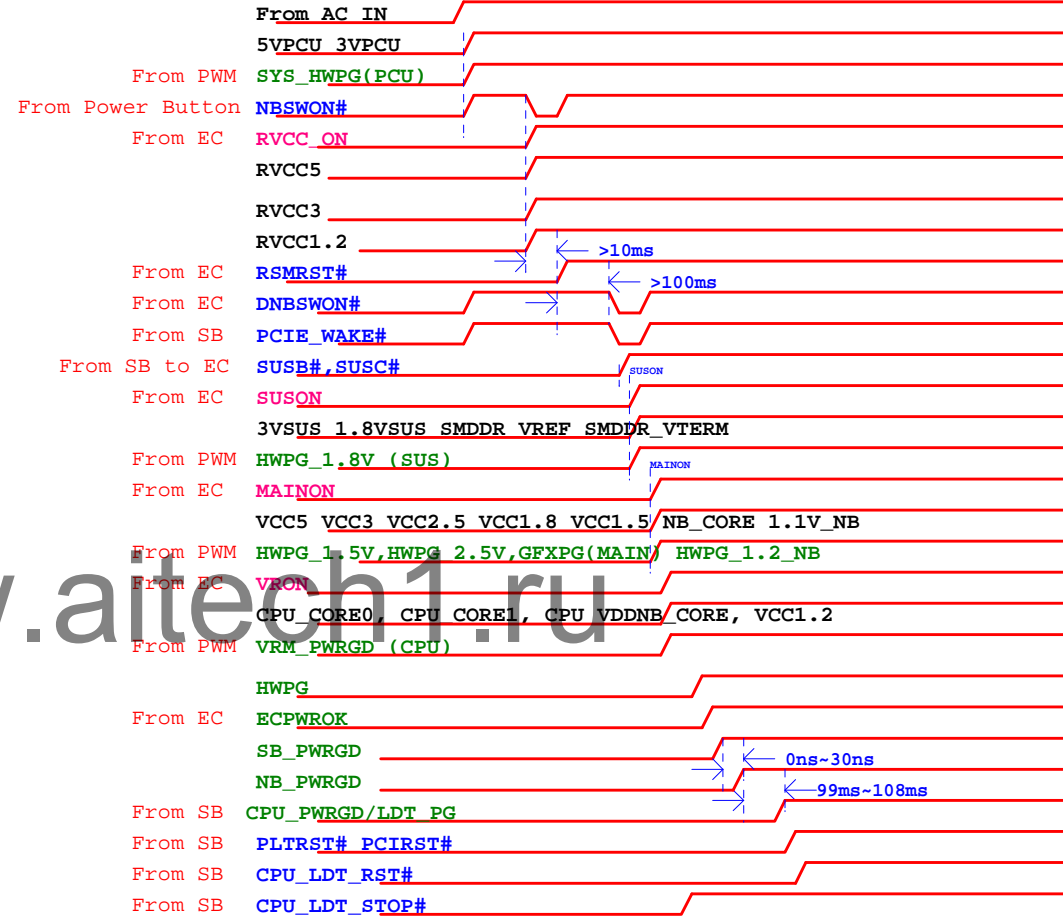
LAYER 1 : TOP
LAYER 2 : VCC
LAYER 3 : IN1
LAYER 4 : IN2
LAYER 5 : GND
LAYER 6 : BOT

Voltage Rails

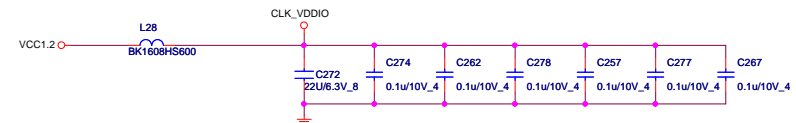
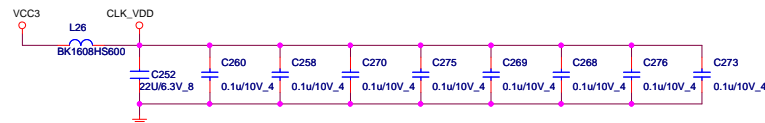
Power	Voltage	S0-S2	S3	S4	S5	Ctl Signal
15VPCU	15V	V	V	V	V	
5VPCU	5V	V	V	V	V	VIN
3VPCU	3V	V	V	V	V	VIN
RVCC3	3V	V	V	V	V	RVCC_ON
RVCC1.2	1.2V	V	V	V	V	RVCC_ON
5VSUS	5V	V	V			SUSD
1.8VSUS	1.8V	V	V			SUSON
VCC5	5V	V				MAIND
VCC3	3V	V				MAIND
VCC1.8	1.8V	V				MAIND
VCC1.5	1.5V	V				MAINON
VCC1.2	1.2V	V				MAINON
CPU_VDDA	2.5V	V				VCC3
NB_CORE	1.2V	V				VRON
SMDDR_VTERM	0.9V	V				SUSON
CPU_CORE	By CPU	V				VR_ON



Power On Sequence

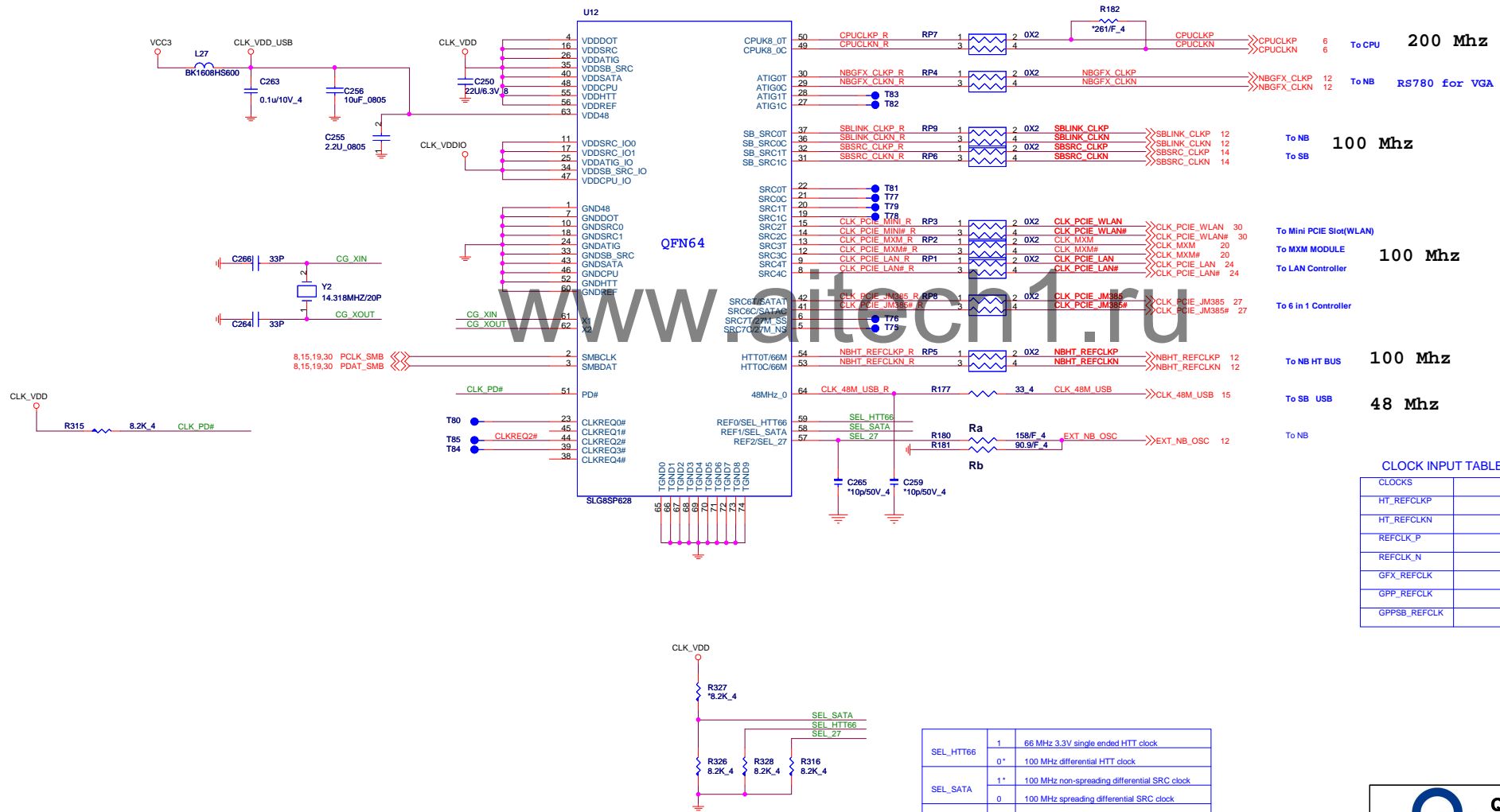


CLK_GEN_SLG8SP628



Place within 0.5" of CLKGEN

ICS9LPRS480	P/N : ALPRS480000
SLG8SP628	P/N : AL8SP628000
RTM880N-796	P/N : AL000880000

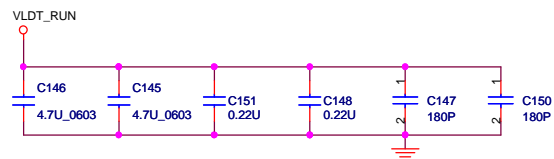
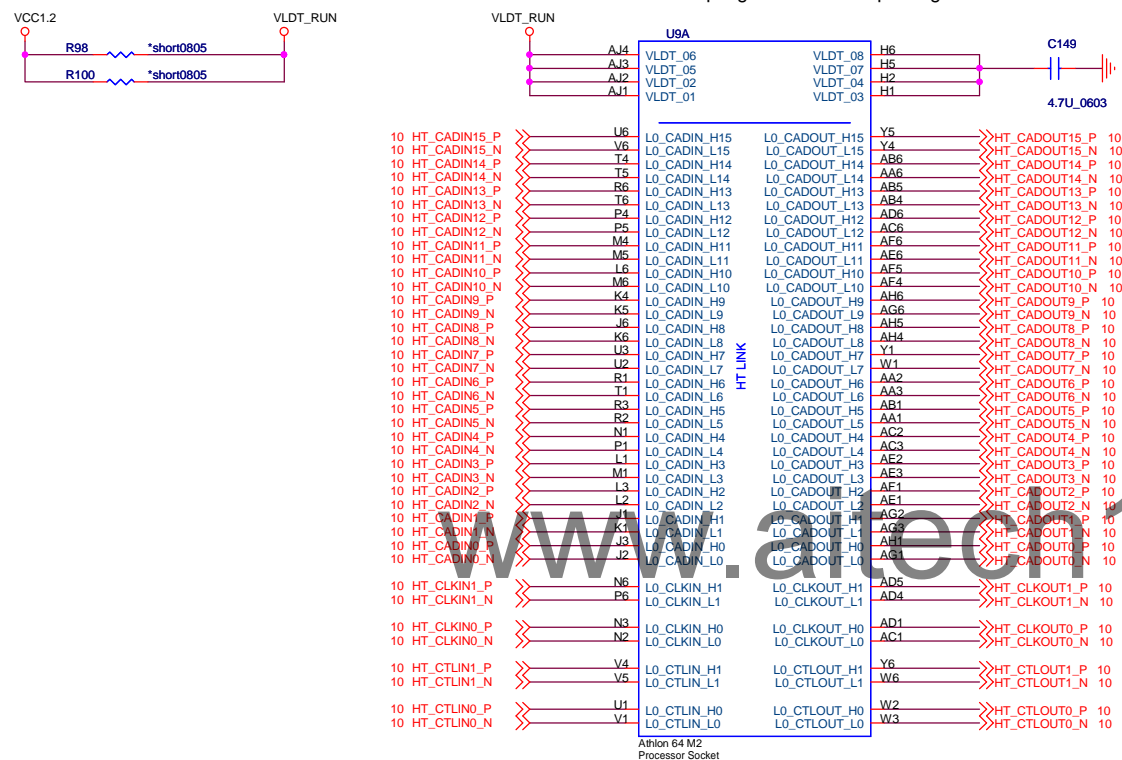


CLOCKS	RS780
HT_REFCLKP	100M DIFF
HT_REFCLKN	100M DIFF
REFCLK_P	14M SE (1.1V)
REFCLK_N	vref
GFX_REFCLK	100M DIFF (IN/OUT)*
GPP_REFCLK	NC or 100M DIFF OUTPUT
GPPSB_REFCLK	100M DIFF

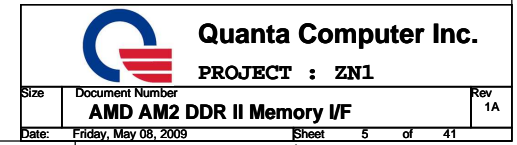
SEL_HTT66	1	66 MHz 3.3V single ended HTT clock
	0*	100 MHz differential HTT clock
SEL_SATA	1*	100 MHz non-spreading differential SRC clock
	0	100 MHz spreading differential SRC clock
SEL_27	1	27MHz and 27M SS outputs
	0*	100 MHz SRC clock

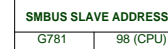
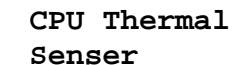
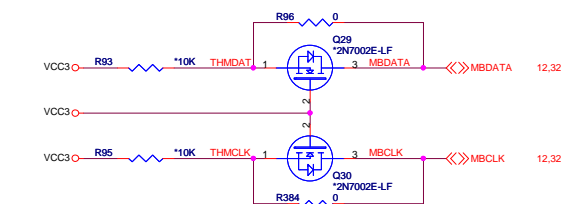
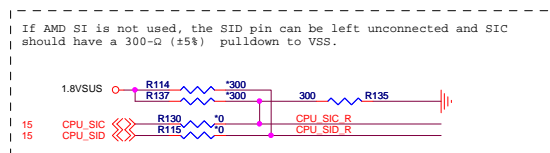
CPU HyperTransport Interface

VDDLTRUNCPU is connected to the VDD_LDT_RUN power supply through the package or on the die. It is only connected on the board to decoupling near the CPU package.

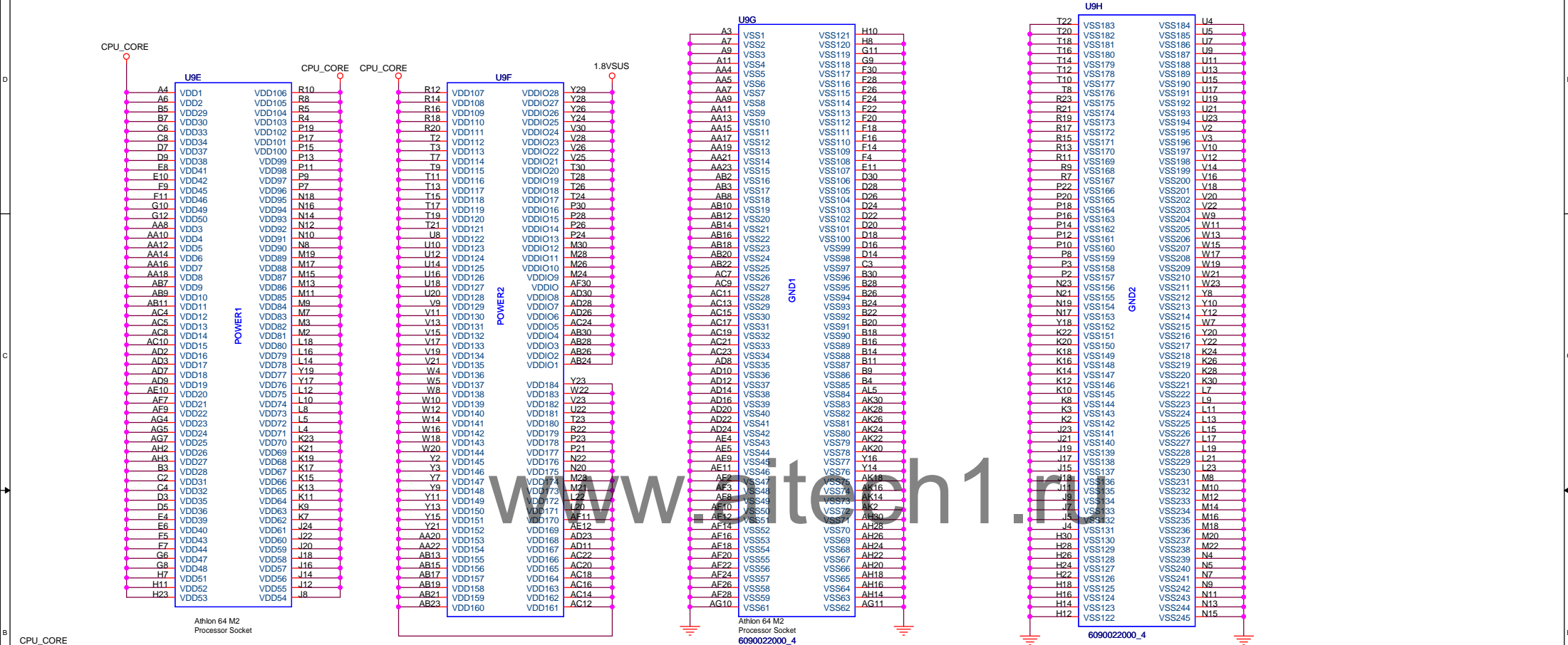


5

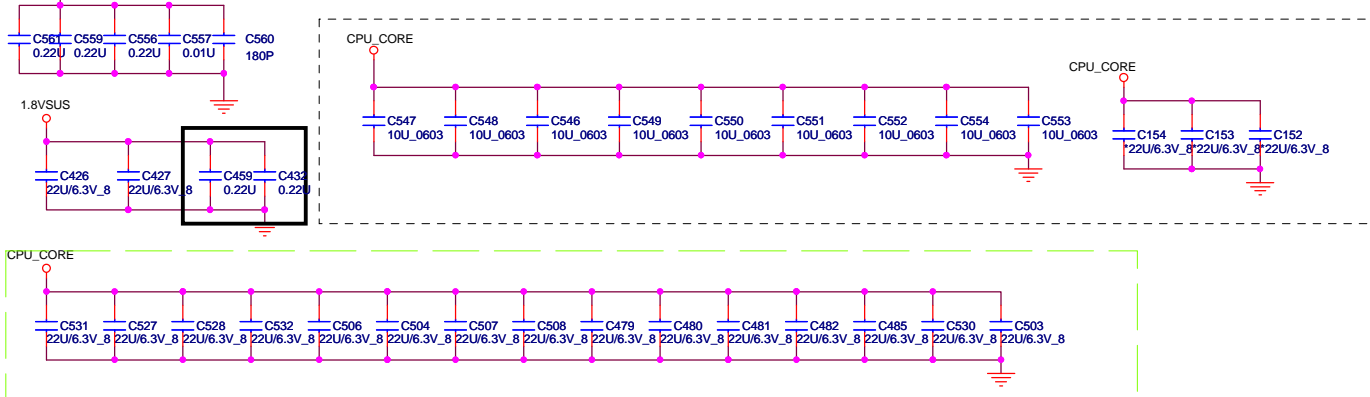




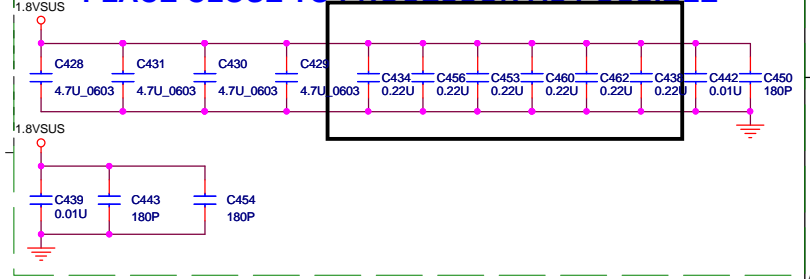
PROCESSOR POWER AND GROUND

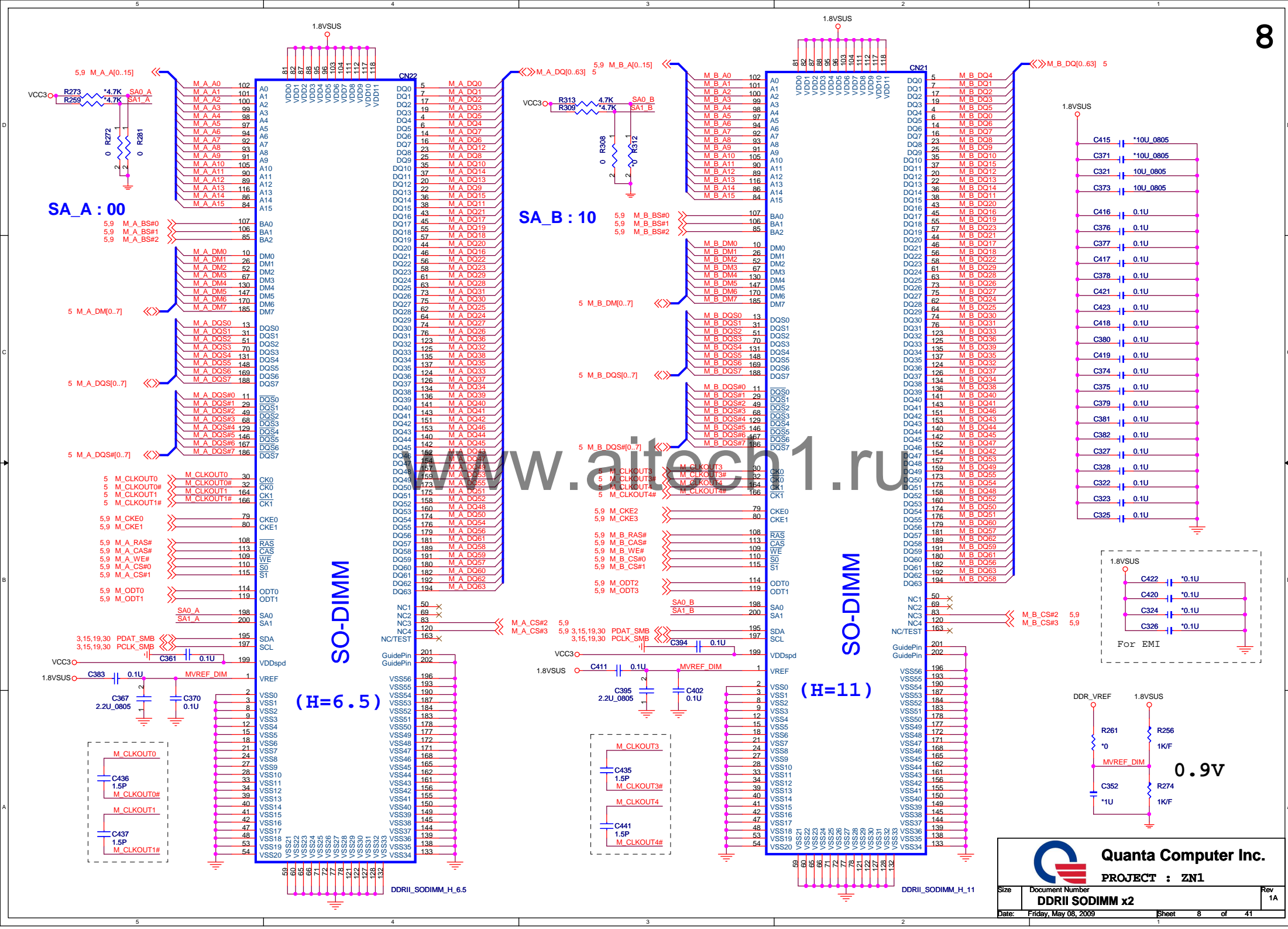


BOTTOMSIDE DECOUPLING



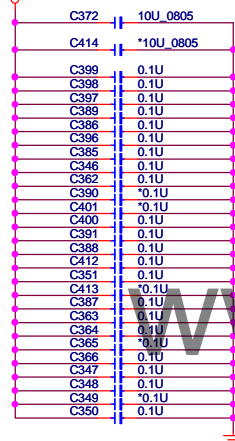
DECOUPLING BETWEEN PROCESSOR AND DIMMs
PLACE CLOSE TO PROCESSOR AS POSSIBLE





0.9V

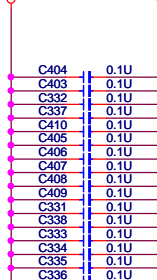
SMDDR_VTERM



1.8VSUS

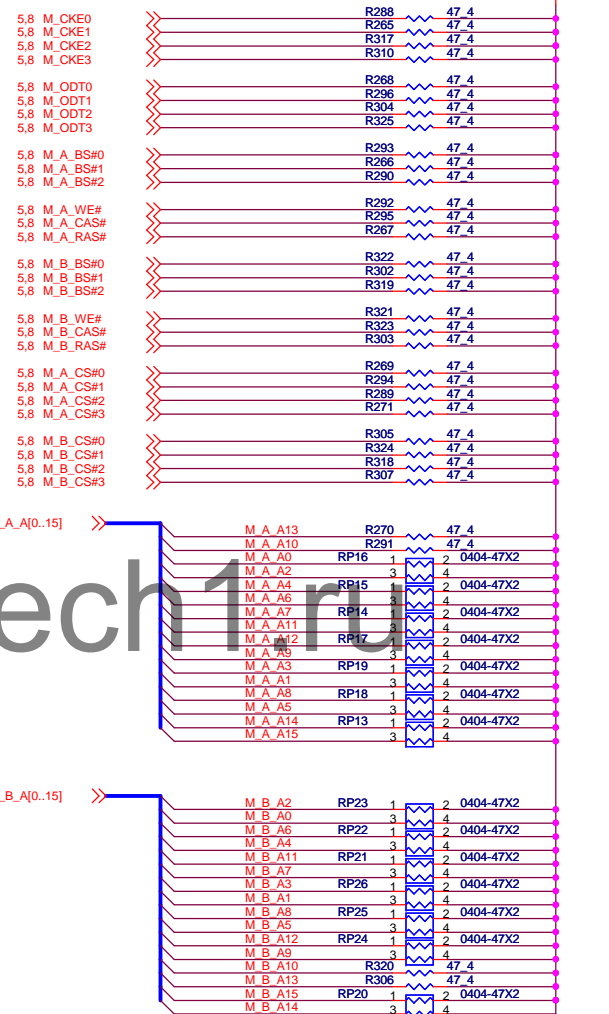
0.9V

SMDDR_VTERM



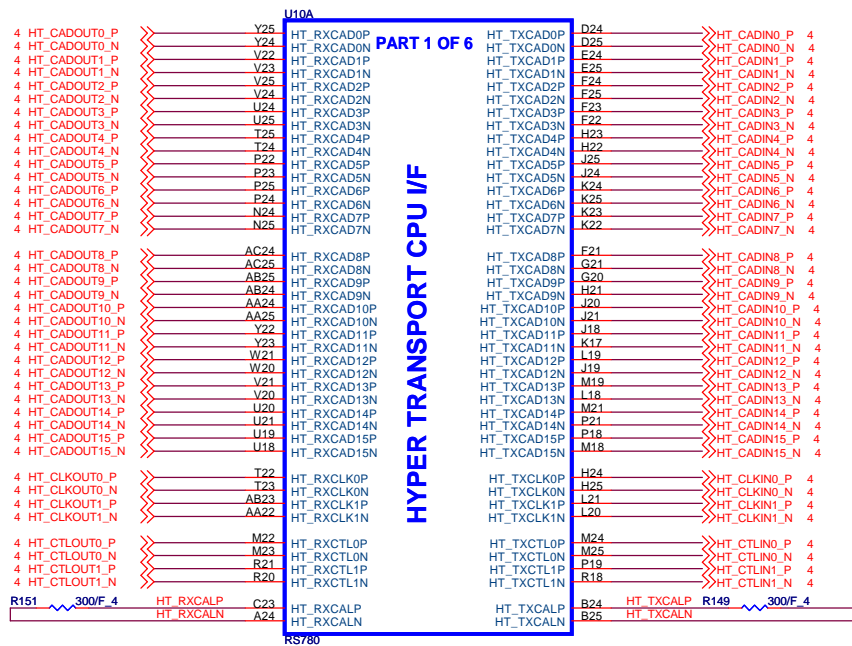
5.8 M_A_A[0..15]

5.8 M_B_A[0..15]



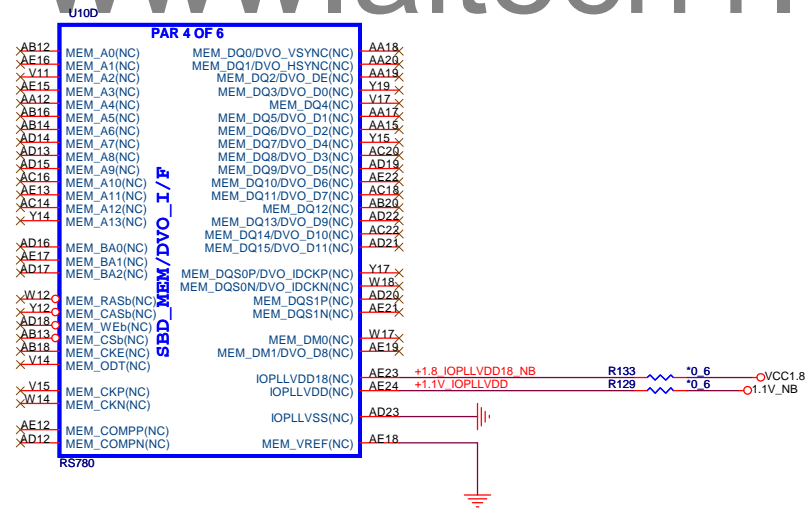
Quanta Computer Inc.

PROJECT : ZN1



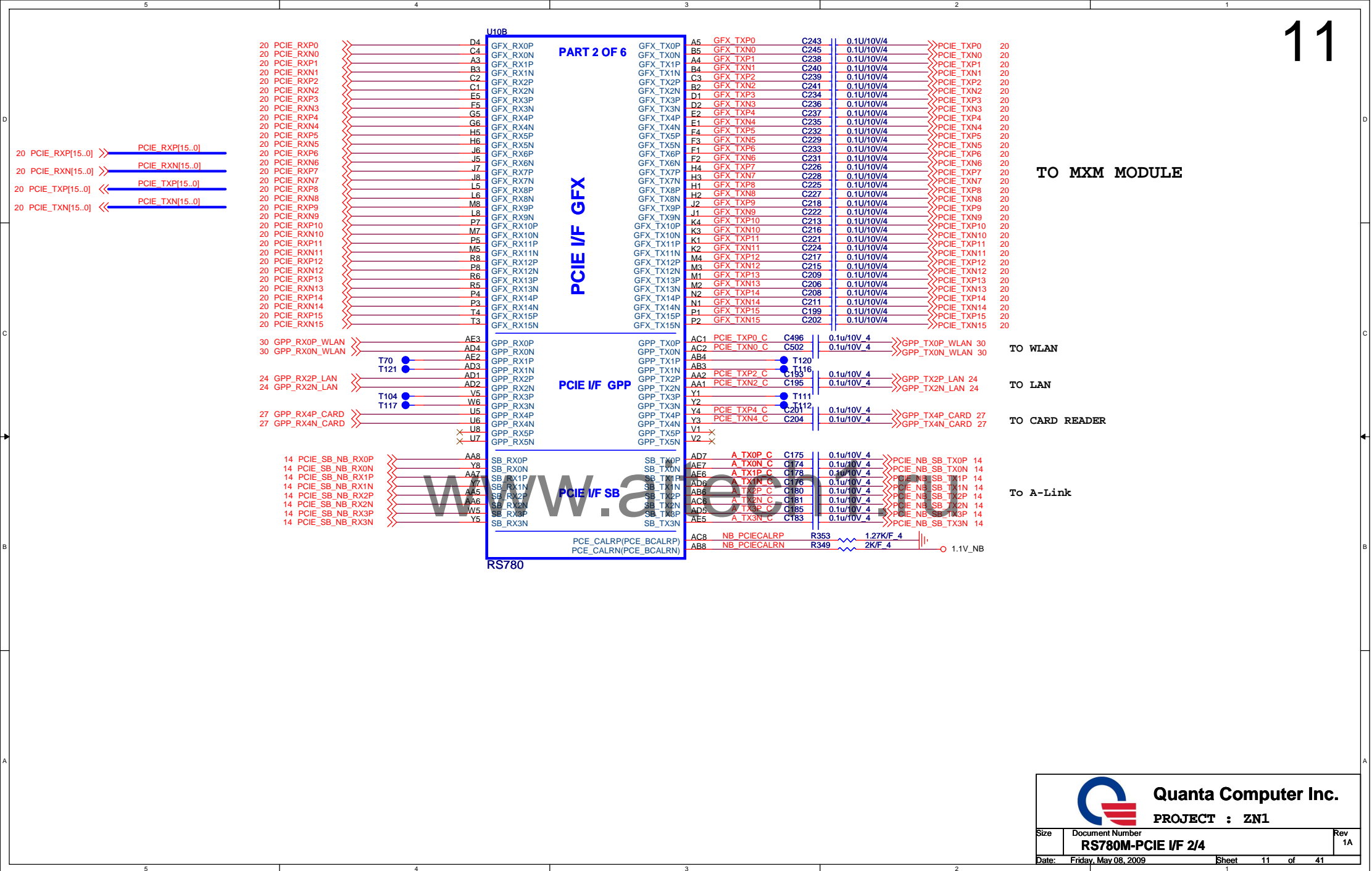
This block is for UMA RS780 only

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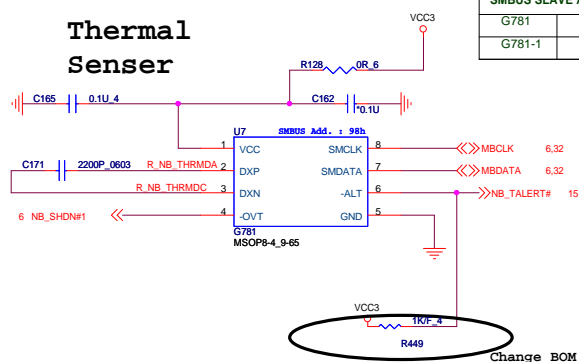


Quanta Computer Inc.

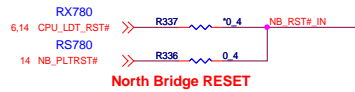
PROJECT : ZN1



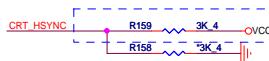
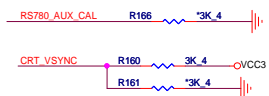
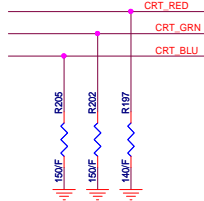
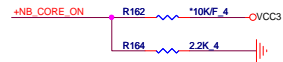
Thermal Sensor



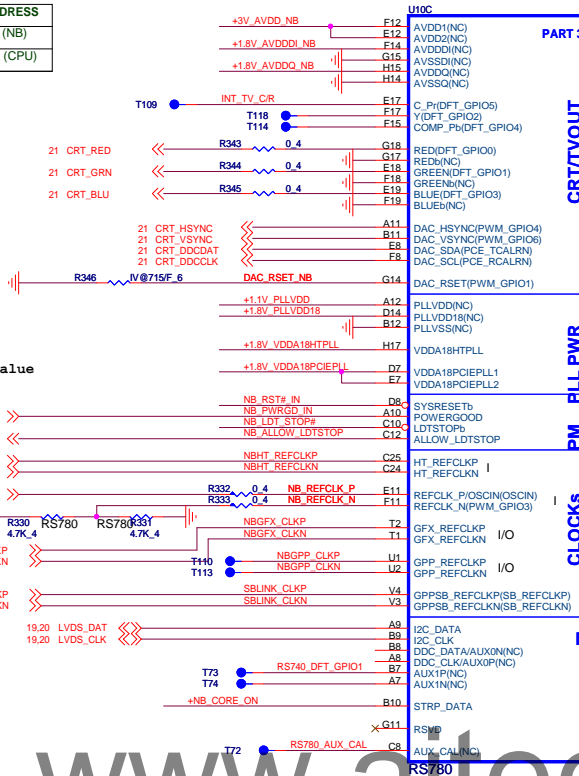
Change BOM value



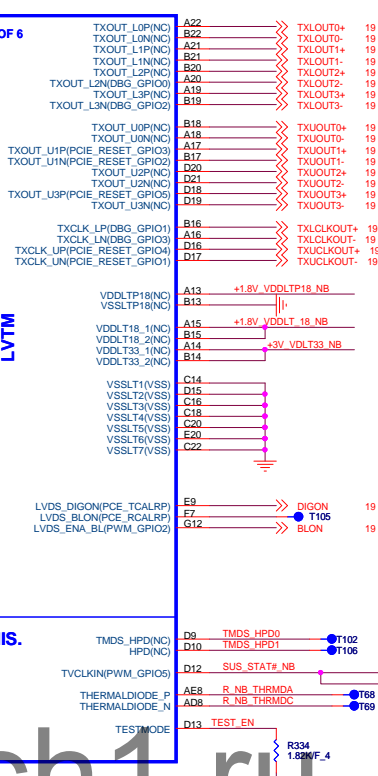
North Bridge RESET



SMBUS SLAVE ADDRESS	
G781	98 (NB)
G781-1	9A (CPU)

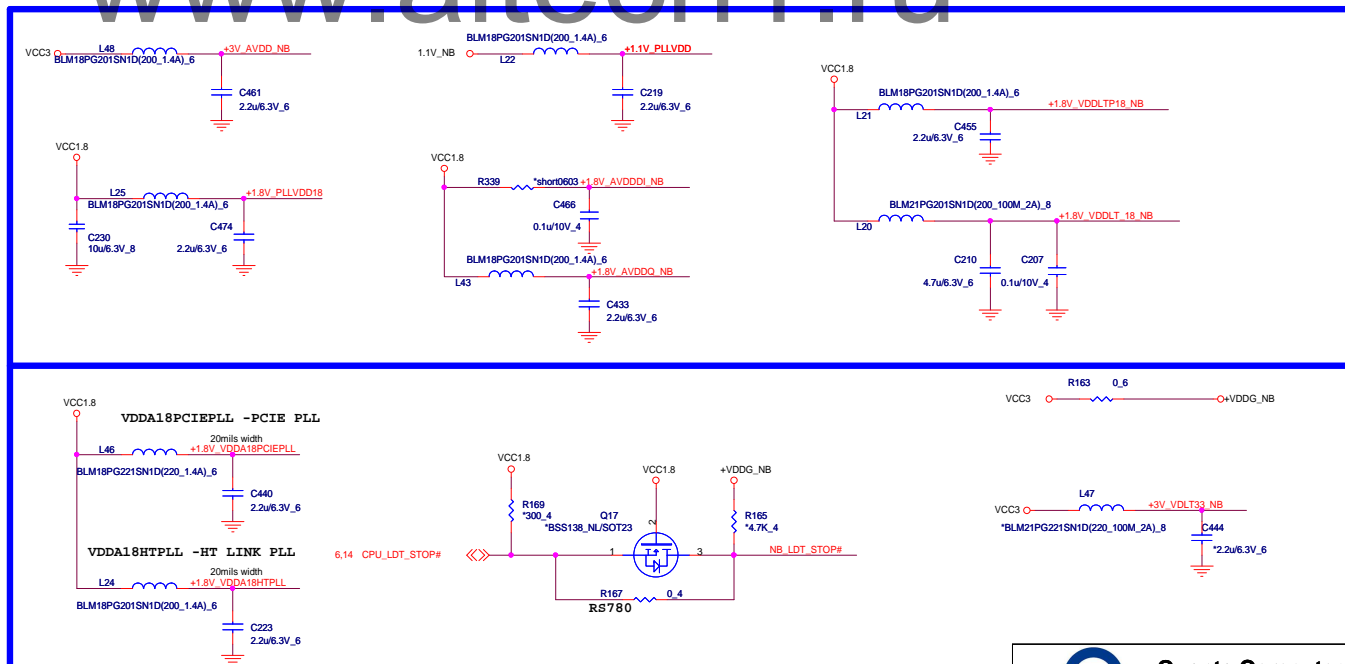


PART 3 OF 6



To LVDS panel

LVDS POWER

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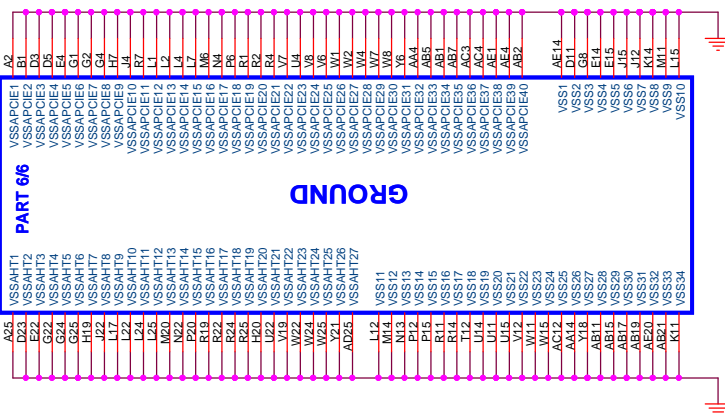
PROJECT : ZN1

Document Number	Rev
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RS780M-SYSTEM I/F 3/4

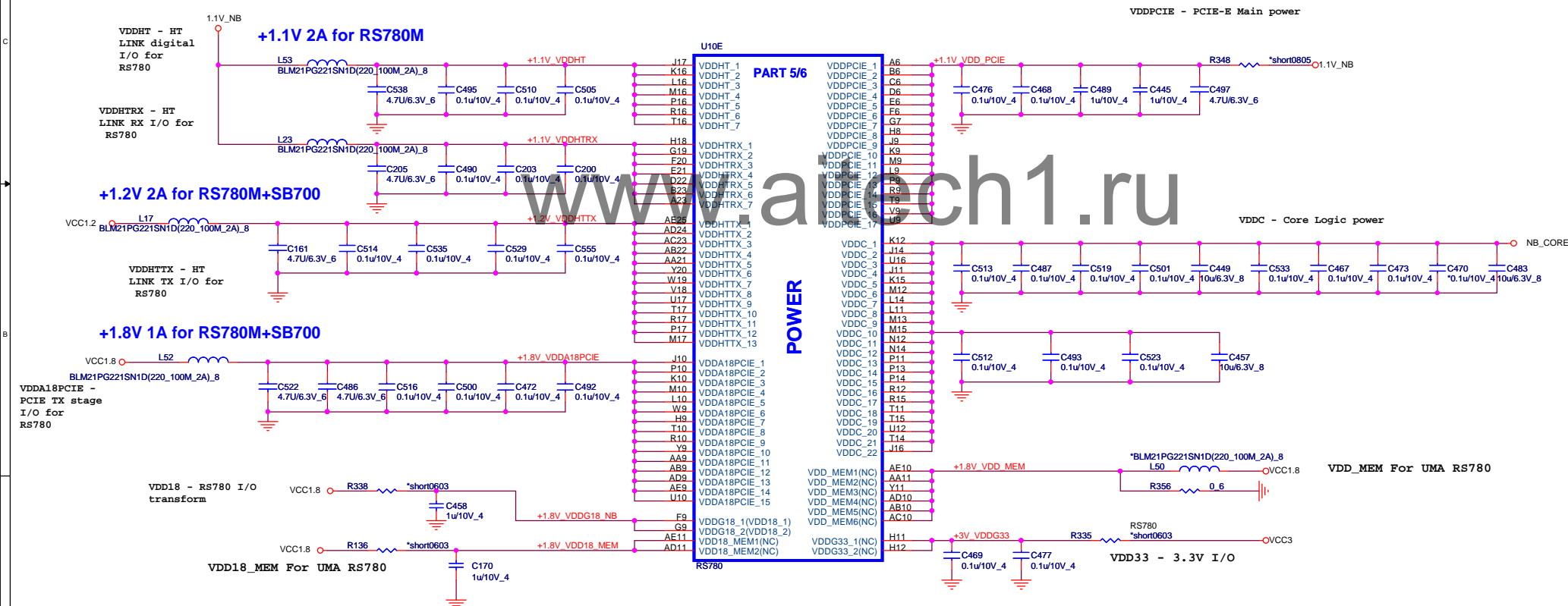
Date: Friday, May 08, 2009 Sheet 12 of 41

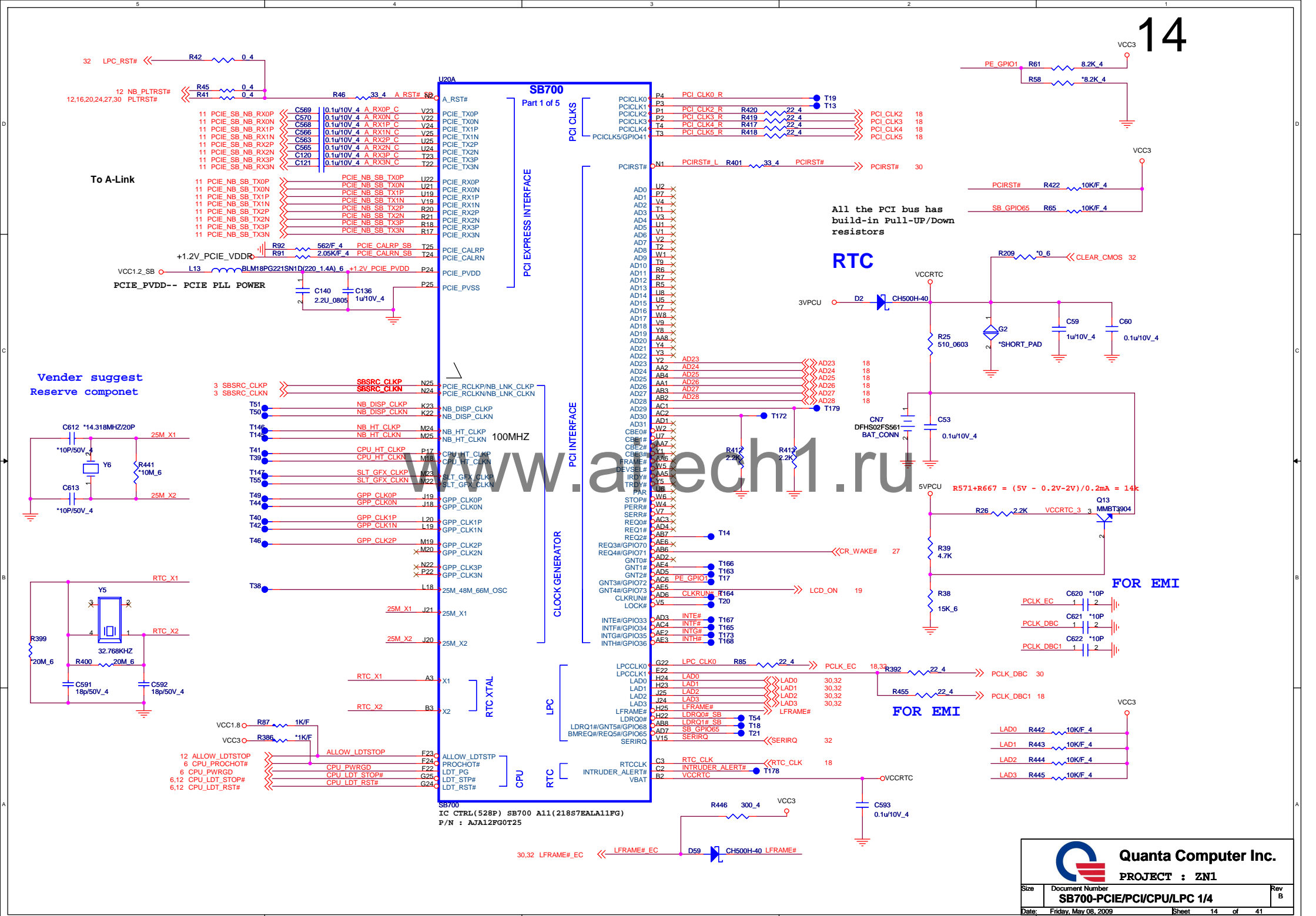
U10F

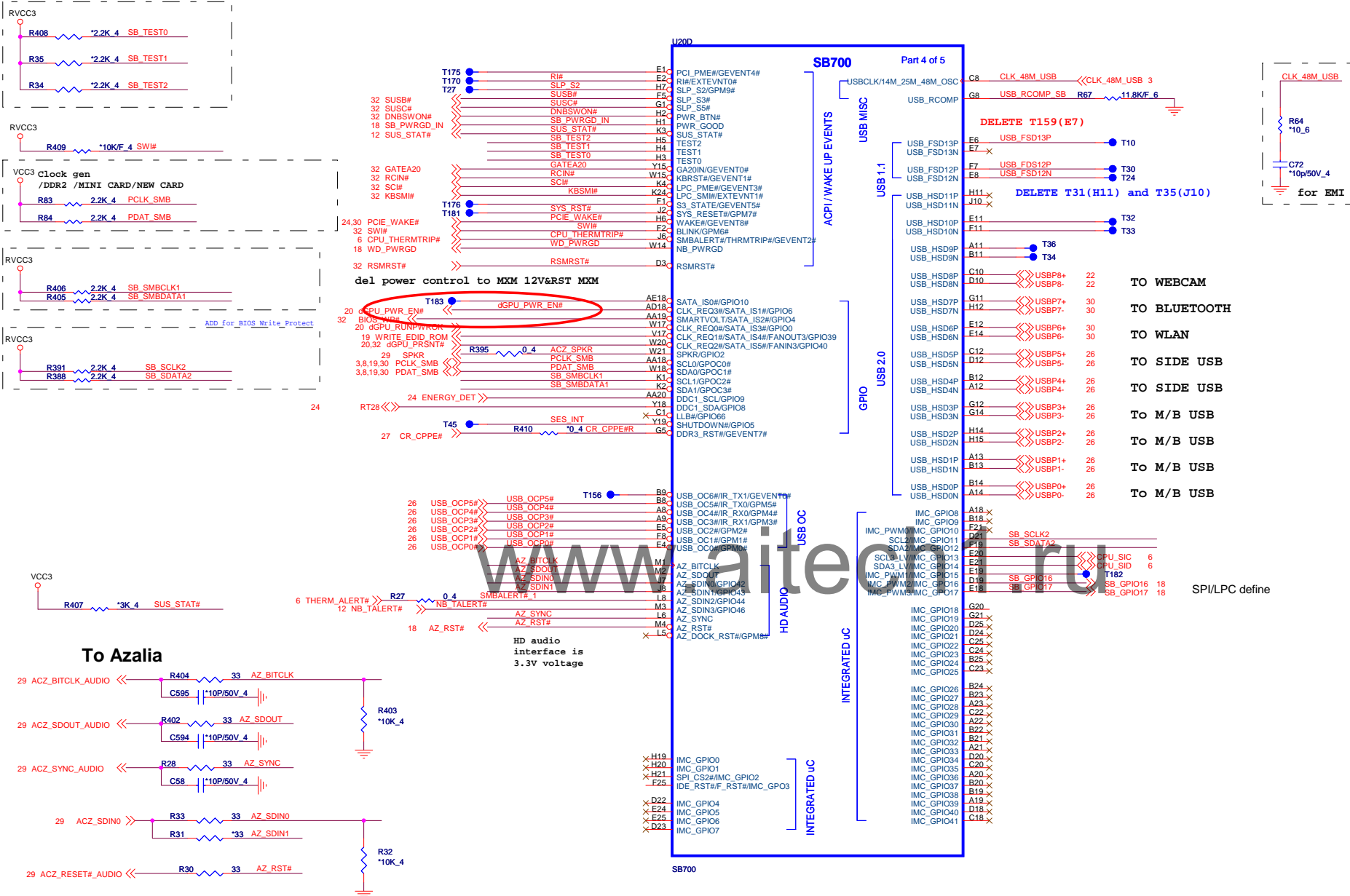


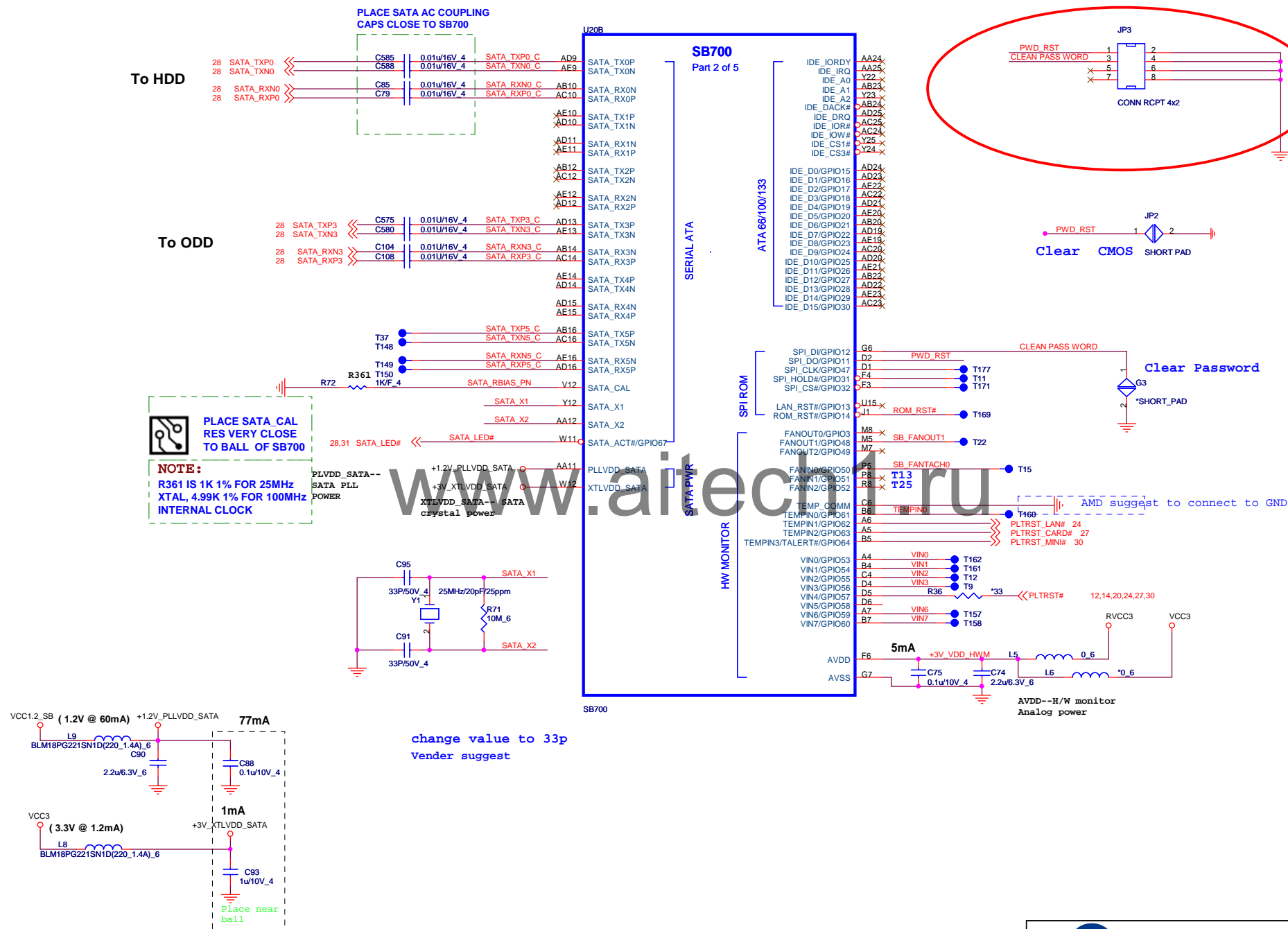
RS780 POWER DIFFERENCE TABLE

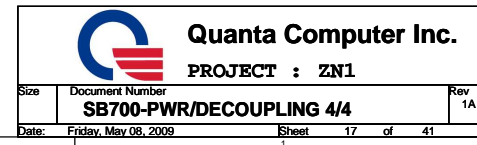
PIN NAME	RS780	PIN NAME	RS780
VDDHT	+1.1V	IOPLLVD	+1.1V
VDDHTRX	+1.1V	AVDD	+3.3V
VDDHTTX	+1.2V	AVDDI	+1.8V
VDDA18PCIE	+1.8V	AVDDQ	+1.8V
VDDG18	+1.8V	PLLVD	+1.1V
VDD18_MEM	+1.8V	PLLVD18	+1.8V
VDDPCIE	+1.1V	VDDA18PCIEPLL	+1.8V
VDDC	+1.1V	VDDA18HTPLL	+1.8V
VDD_MEM	+1.8V/1.5V	VDDLTP18	+1.8V
VDDG33	+3.3V	VDDL18	+1.8V
IOPLLVD18	+1.8V	VDDL18	NC











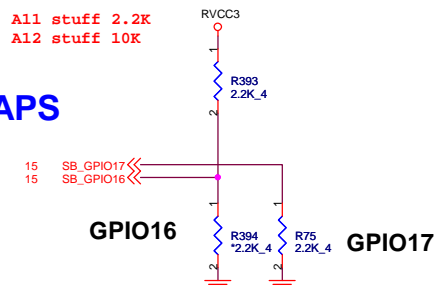


OVERLAP COMMON PADS WHERE
POSSIBLE FOR DUAL-OP RESISTORS.

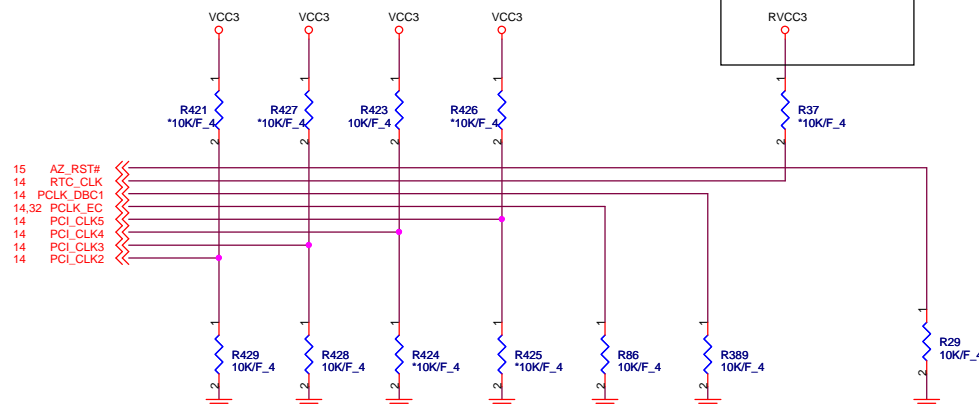
It must ready
before RSMRST#

REQUIRED STRAPS

A11 stuff 2.2K
A12 stuff 10K



TYPE	GPIO16	GPIO17
FWH	L : 2.2K pull down	L : 2.2K pull down
LPC	NC	L : 2.2K pull down
SPI	L : 2.2K pull down	NC
RSVD	NC	NC



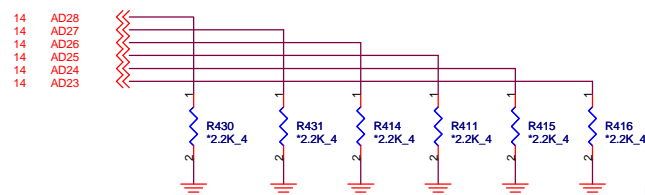
	PCI_CLK2	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLK0	LPC_CLK1	RTC_CLK	AZ_RST#
PULL HIGH	BOOTFAIL TIMER ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	ENABLE PCI MEM BOOT	CLKGEN ENABLED	INTERNAL RTC DEFAULT	EC ENABLED
PULL LOW	BOOTFAIL TIMER DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			DISABLE PCI MEM BOOT DEFAULT	CLKGEN DISABLED DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	EC DISABLED DEFAULT

EC
ENABLED

ENABLE PCI
MEM BOOT

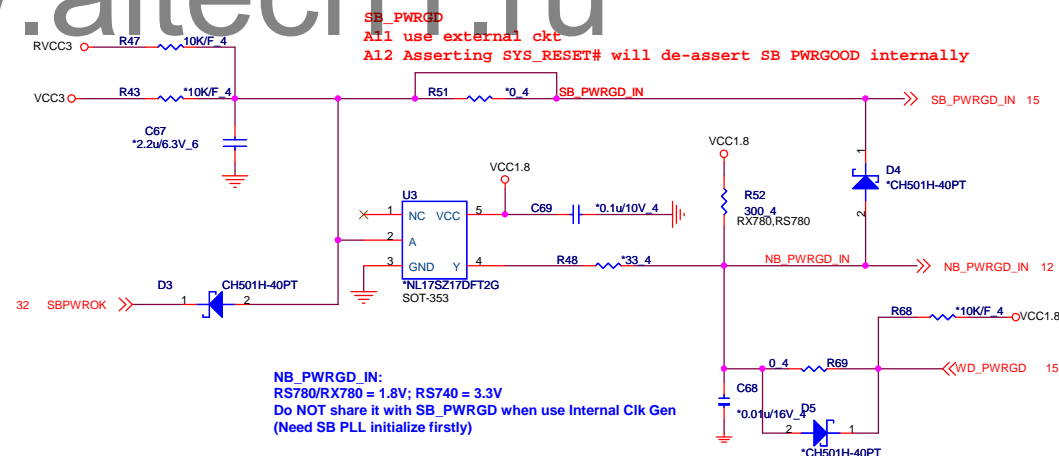
DEBUG STRAPS

SB700 HAS 15K INTERNAL PU FOR PCI_AD[28:23]



Use 2.2K PD.

	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	RESERVED
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	

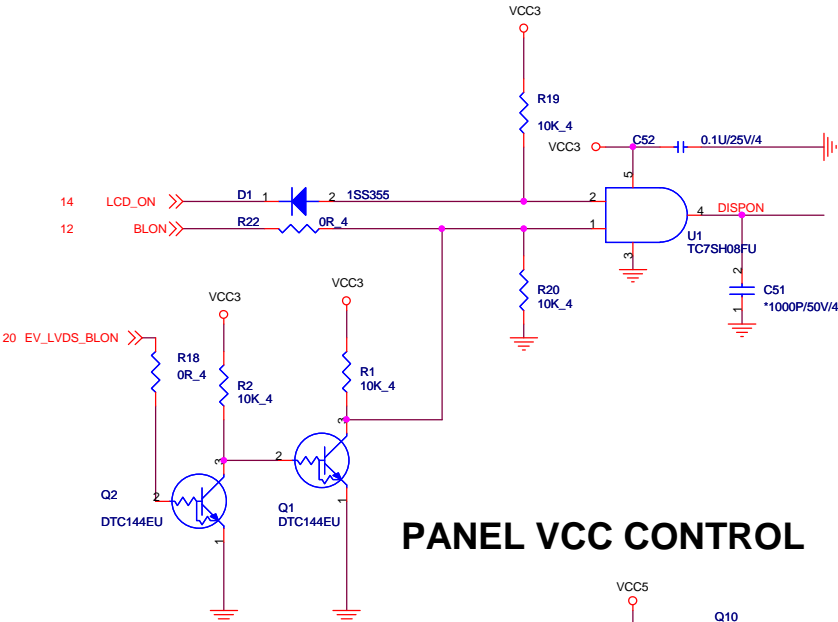


NB_PWRGD_IN:
RS780/RX780 = 1.8V; RS740 = 3.3V
Do NOT share it with SB_PWRGD when use Internal Clk Gen
(Need SB PLL initialize firstly)

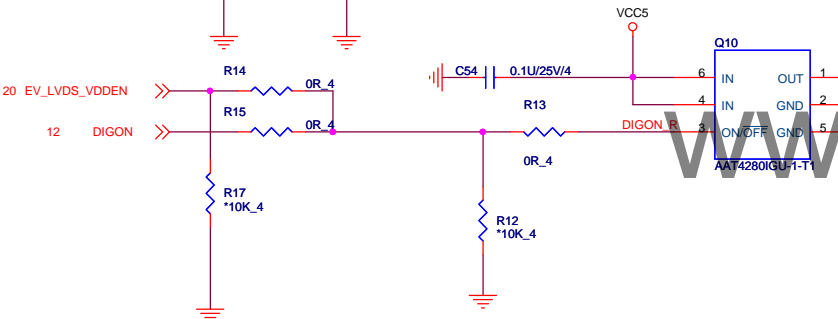


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PROJECT : ZN1

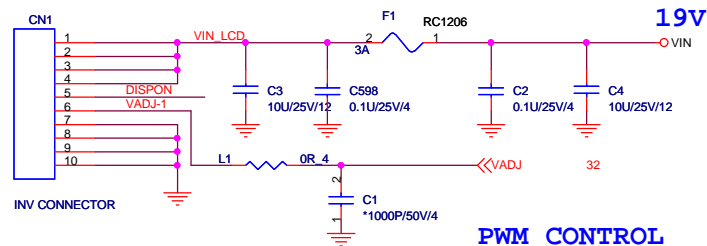
BACKLIGHT CONTROL



PANEL VCC CONTROL

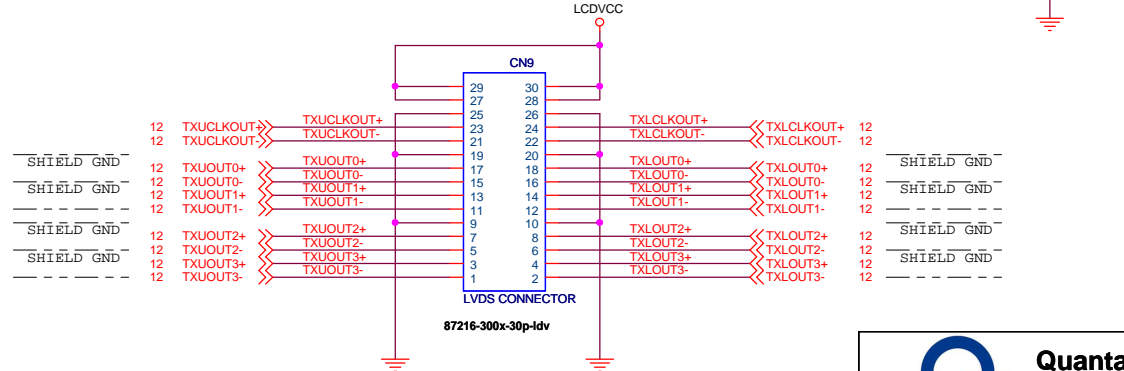


TO INVERTER POWER

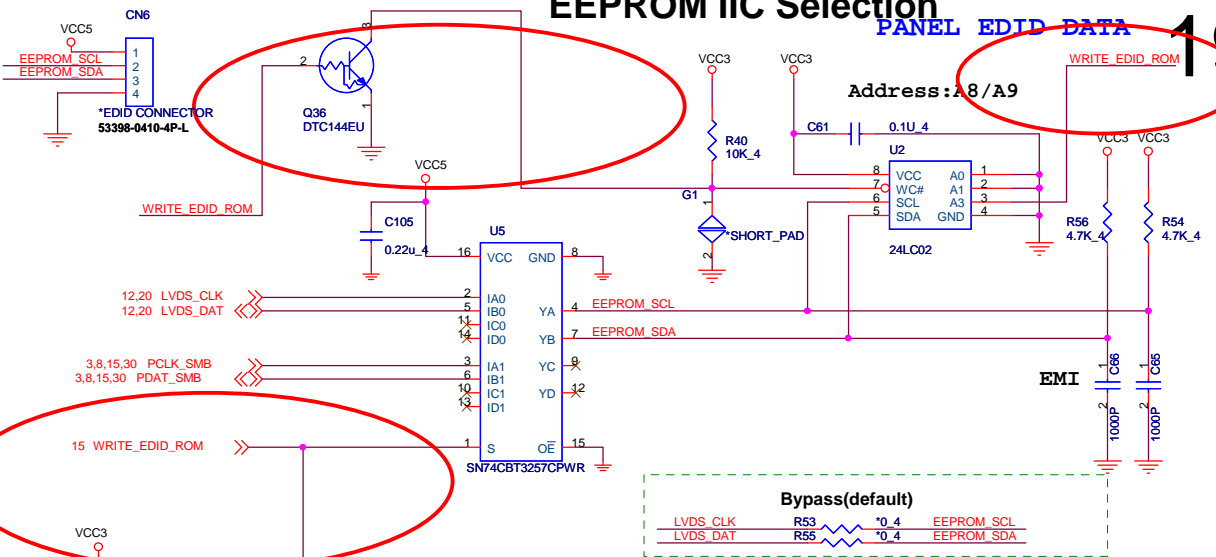


PWM CONTROL

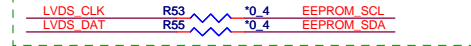
LCD PANEL CONNECTOR



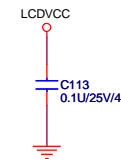
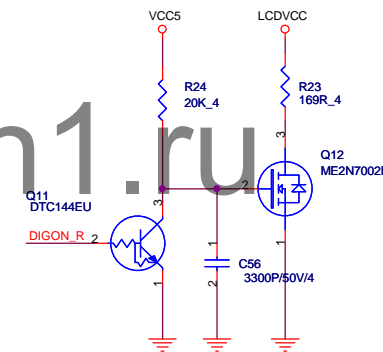
EEPROM IIC Selection



Bypass(default)



Discharge panel power

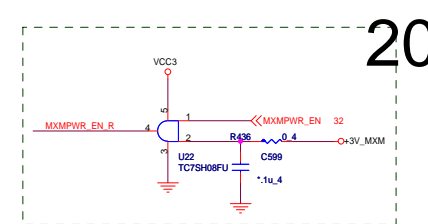
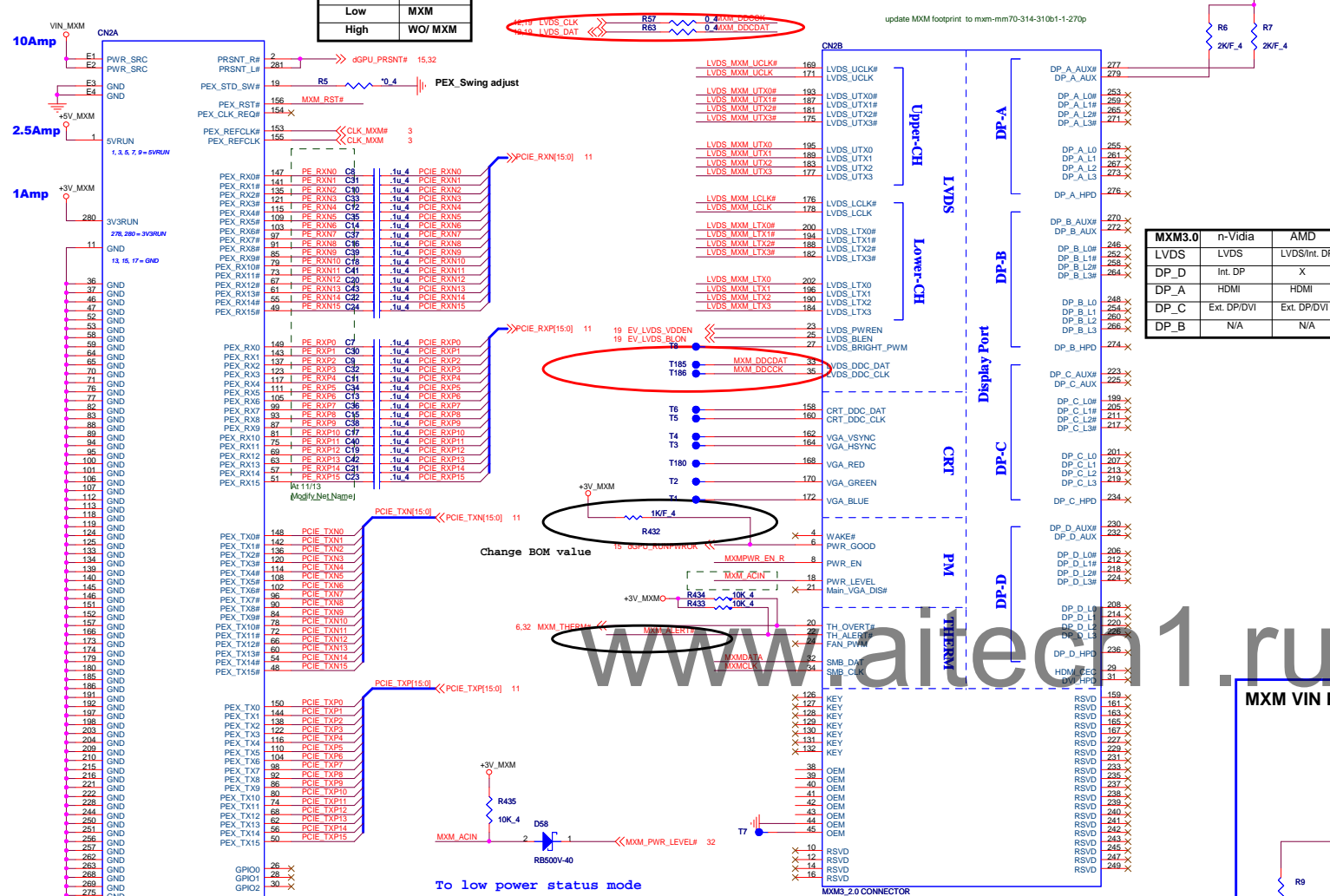


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PROJECT : ZN1

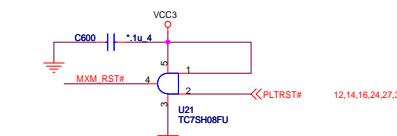
MXM Module

dGPU_PRSENT#	Sku
Low	MXM
High	WO/ MXM

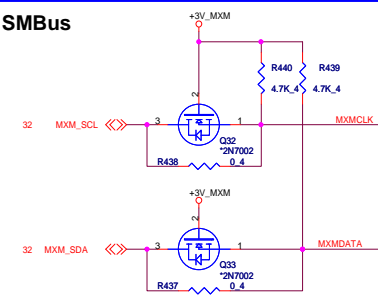


MXM3.0	n-Vidia	AMD
LVDS	LVDS	LVDS/Int. DP
DP_D	Int. DP	X
DP_A	HDMI	HDMI
DP_C	Ext. DP/DVI	Ext. DP/DVI
DP_B	N/A	N/A

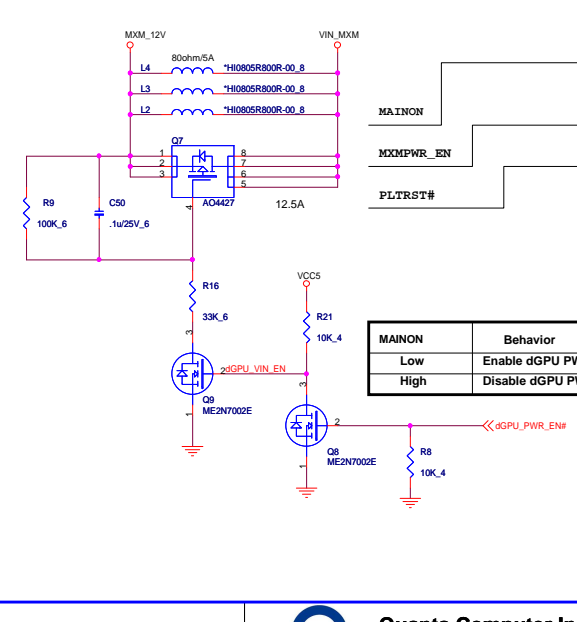
MXM Reset



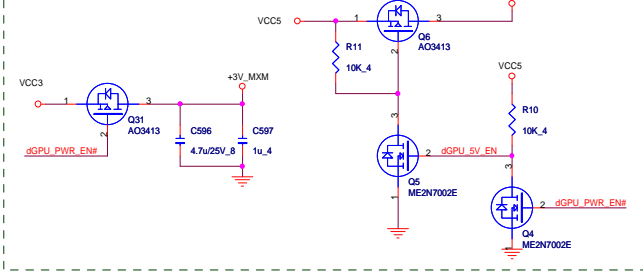
SMBus



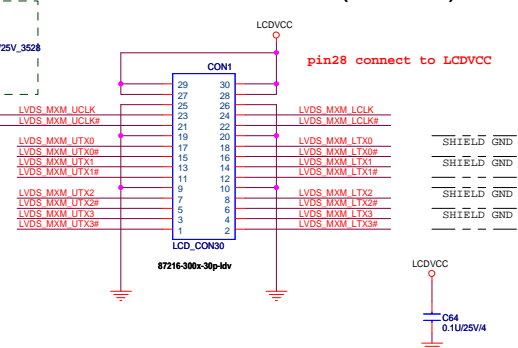
MXM VIN Power switch

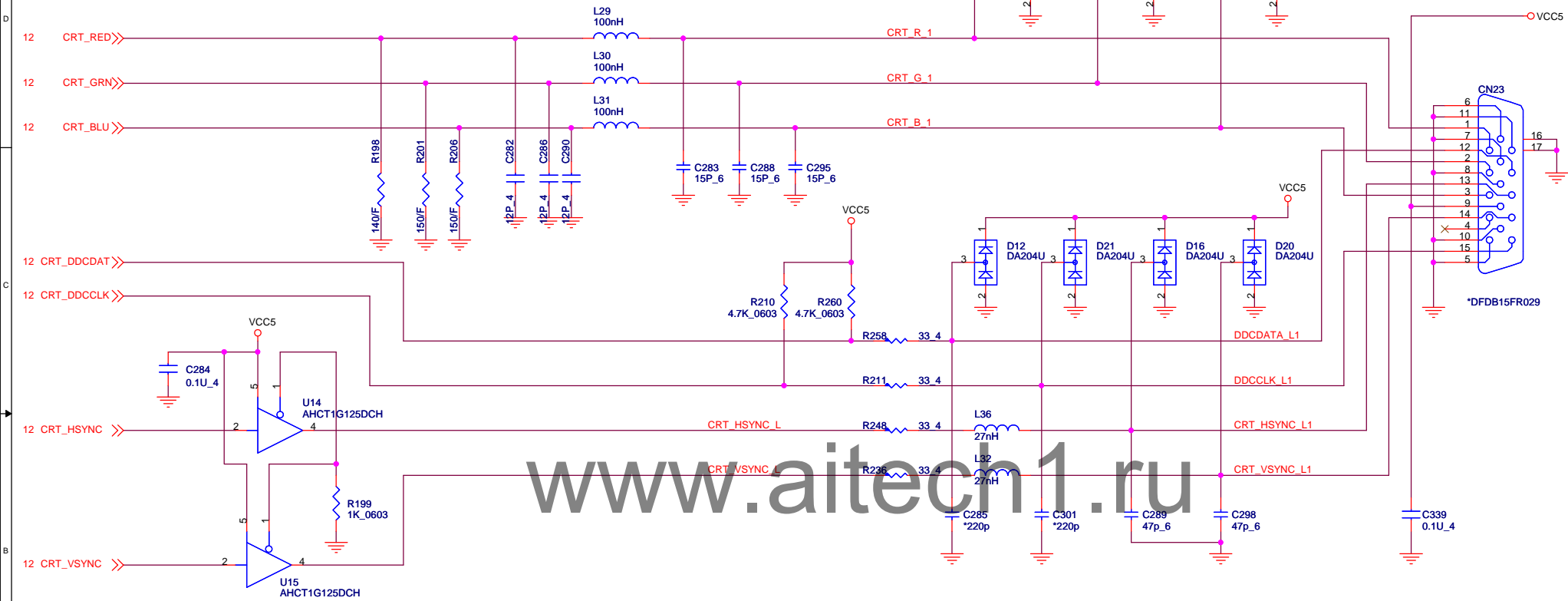


MXM 3V/5V Power switch



LCD PANEL CONNECTOR(WITH MXM



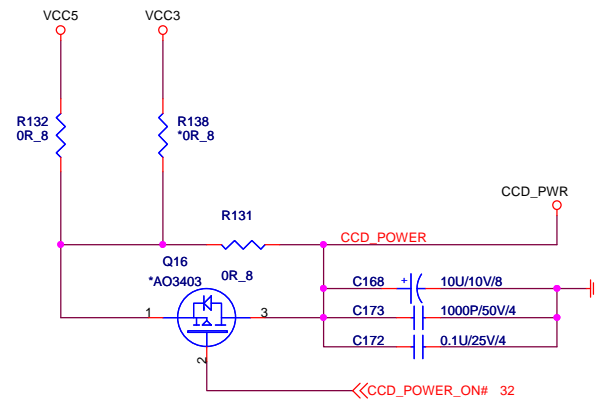


Quanta Computer Inc.

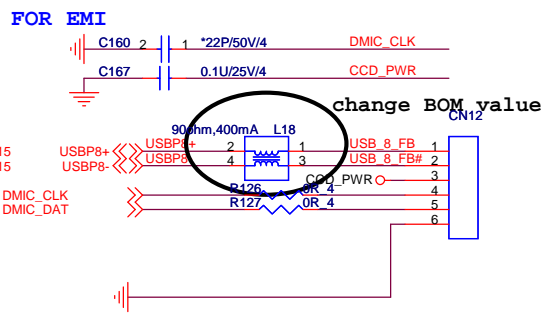
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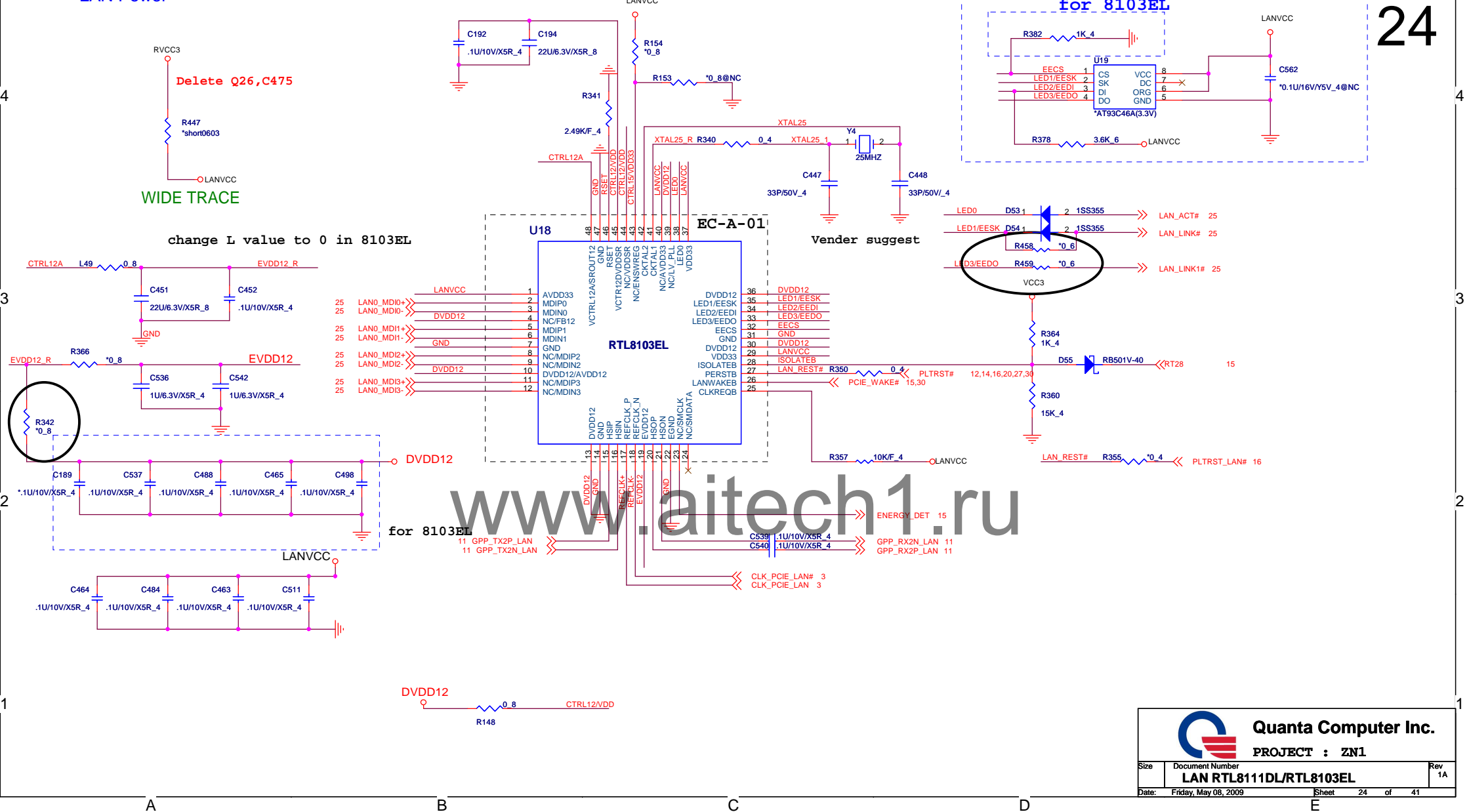
Size	Document Number	Rev
	CRT (Reserved for Debug only)	1A
Date:	Friday, May 08, 2009	Sheet 21 of 41

CAMERA POWER CONTROL



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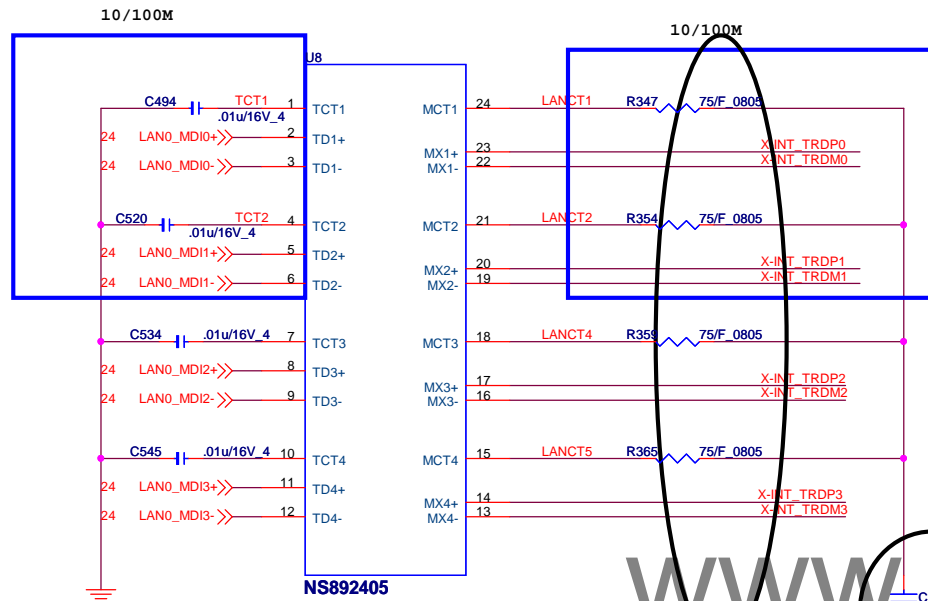


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PROJECT : ZN1

Size	Document Number	Rev
	LAN RTL8111DL/RTL8103EL	1A

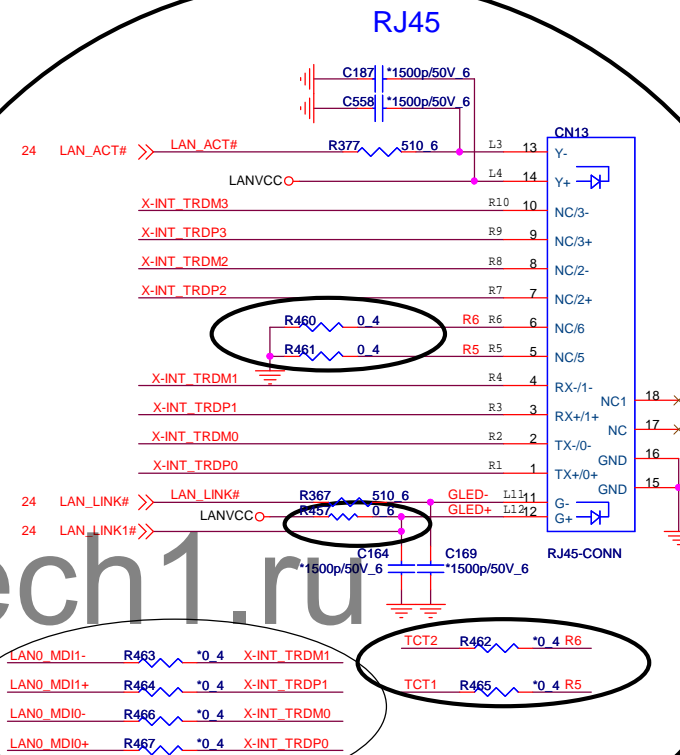
Date: Friday, May 08, 2009 Sheet 24 of 41



100/1000 Base T NS892402
10/100 Base T NS892405

change the footprint and BOM

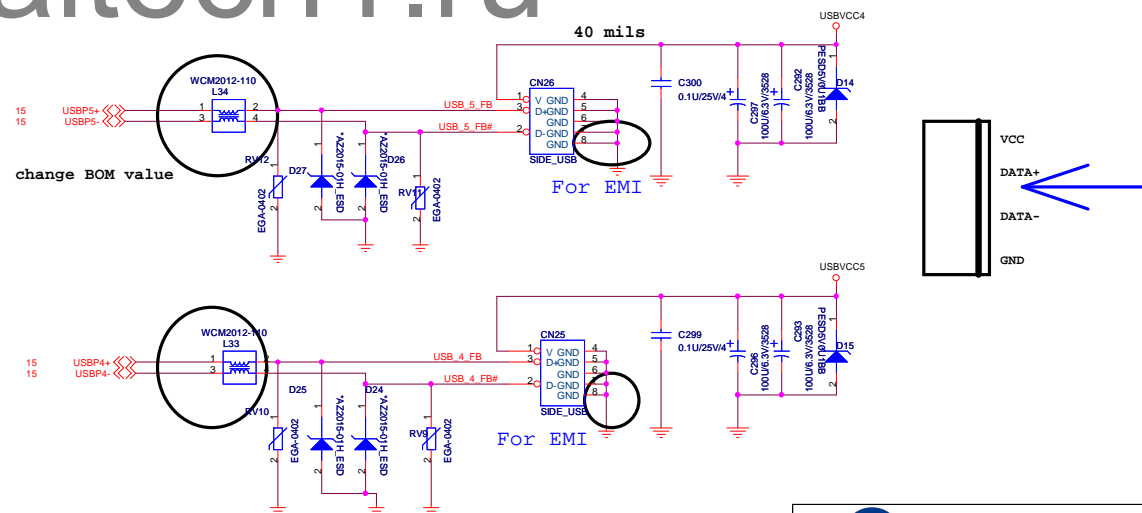
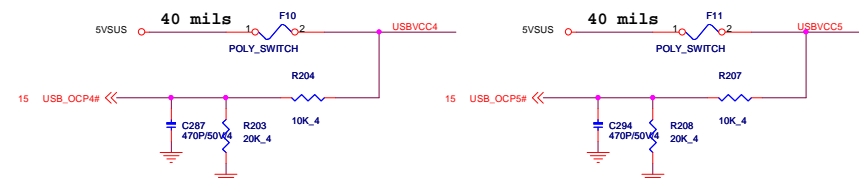
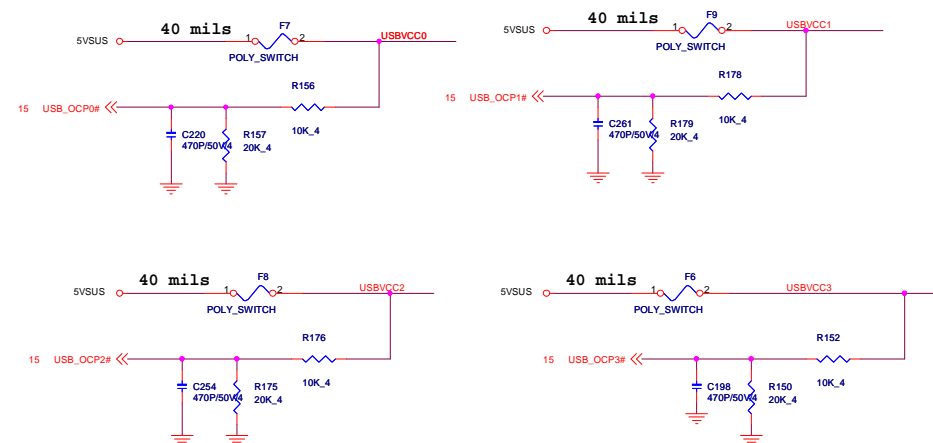
delete RV1-RV8



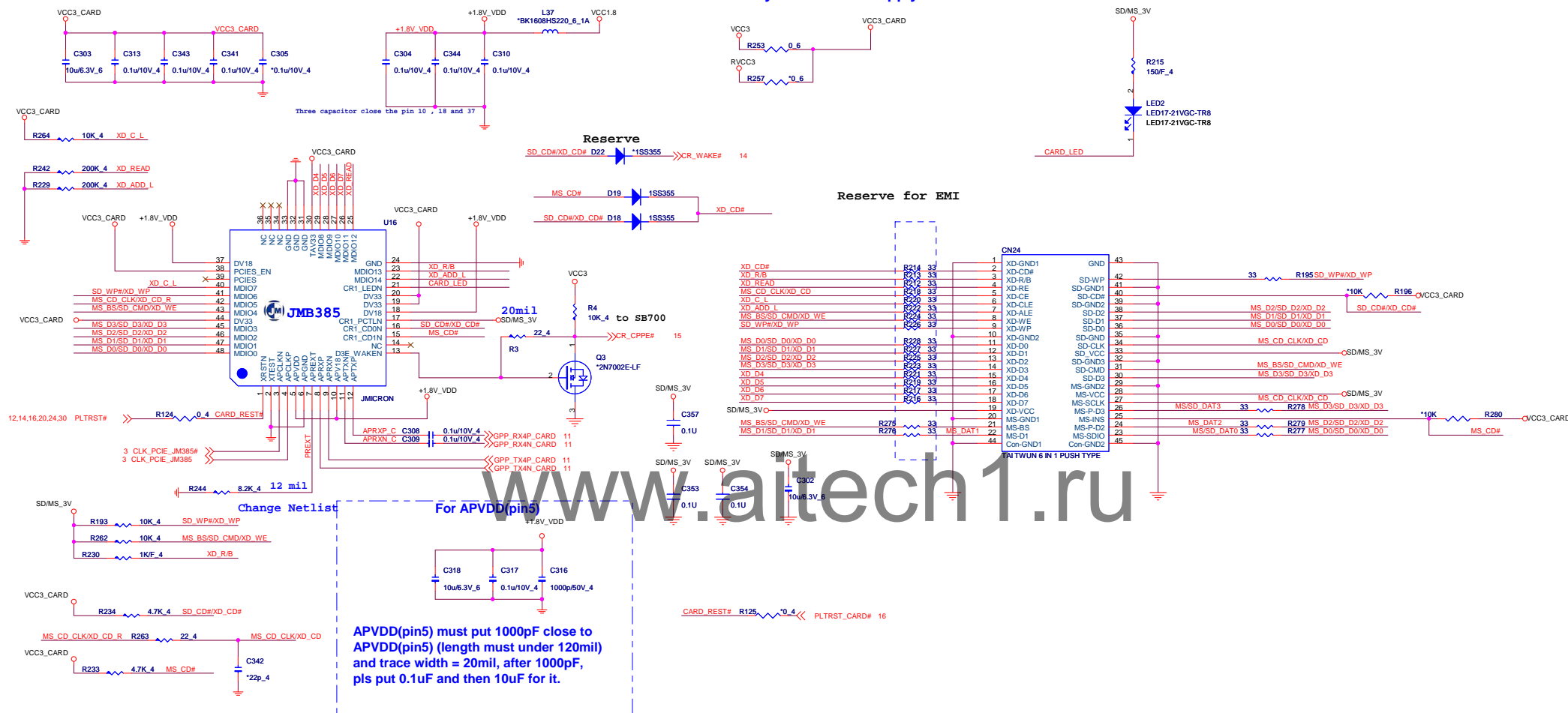
Quanta Computer Inc.

PROJECT : ZN1

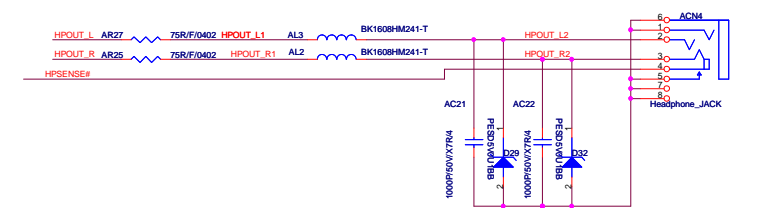
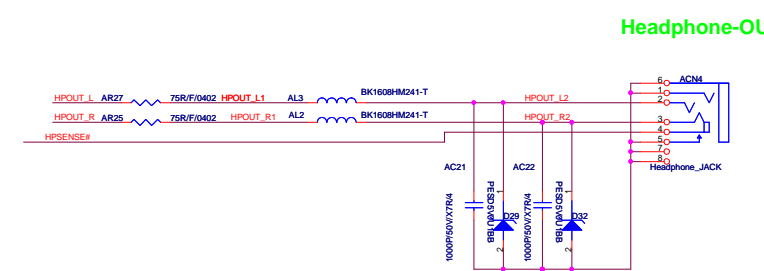
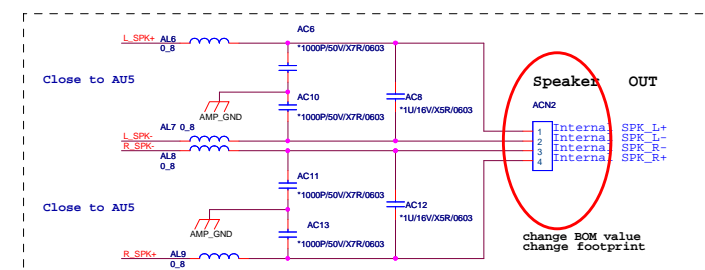
Size	Document Number	Rev
	LAN Transformer & RJ45	1A
Date:	Friday, May 08, 2009	Sheet 25 of 41



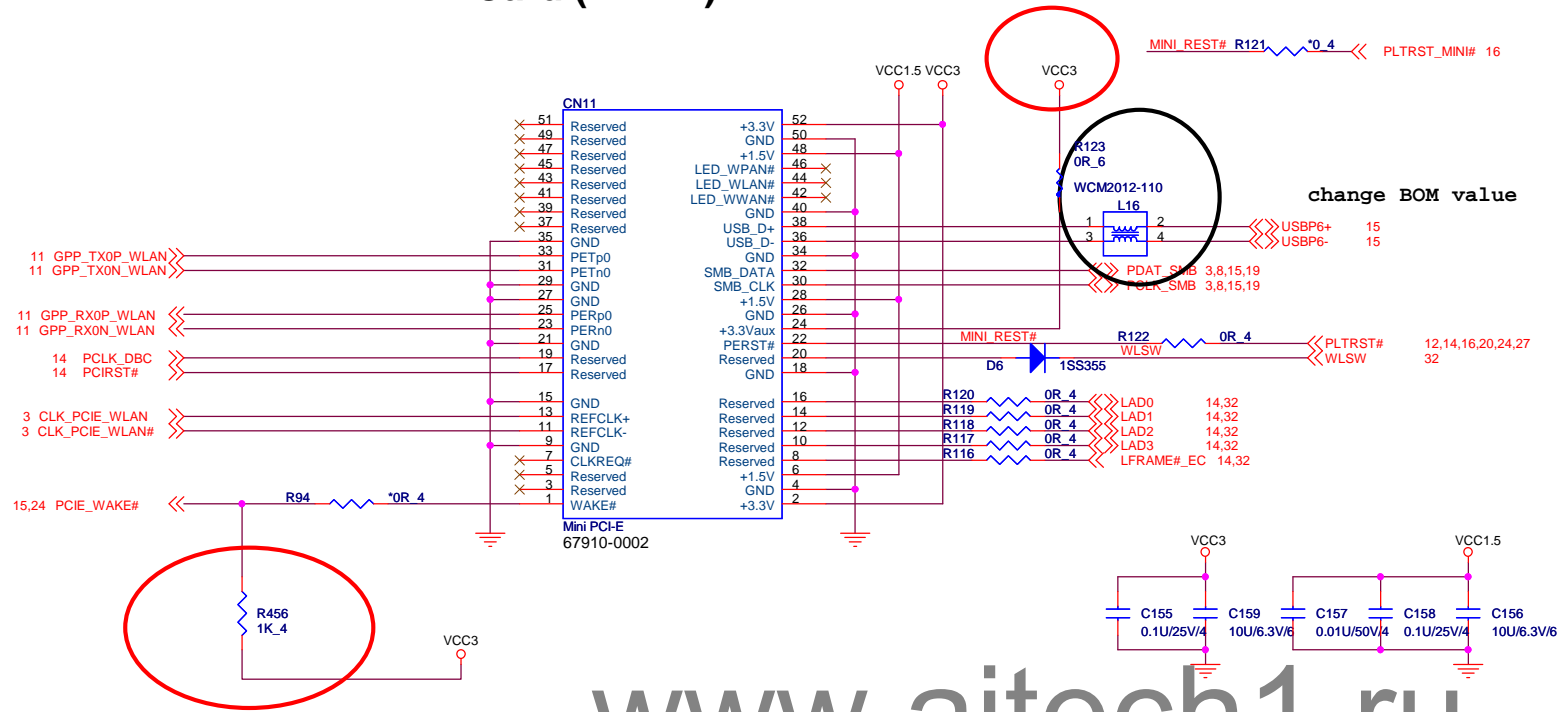
Memory Card Power Supply



APVDD(pin5) must put 1000pF close to APVDD(pin5) (length must under 120mil) and trace width = 20mil, after 1000pF, pls put 0.1uF and then 10uF for it.



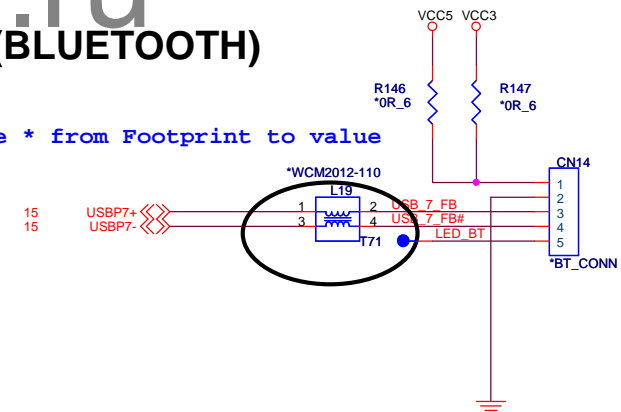
Mini Card (WLAN)



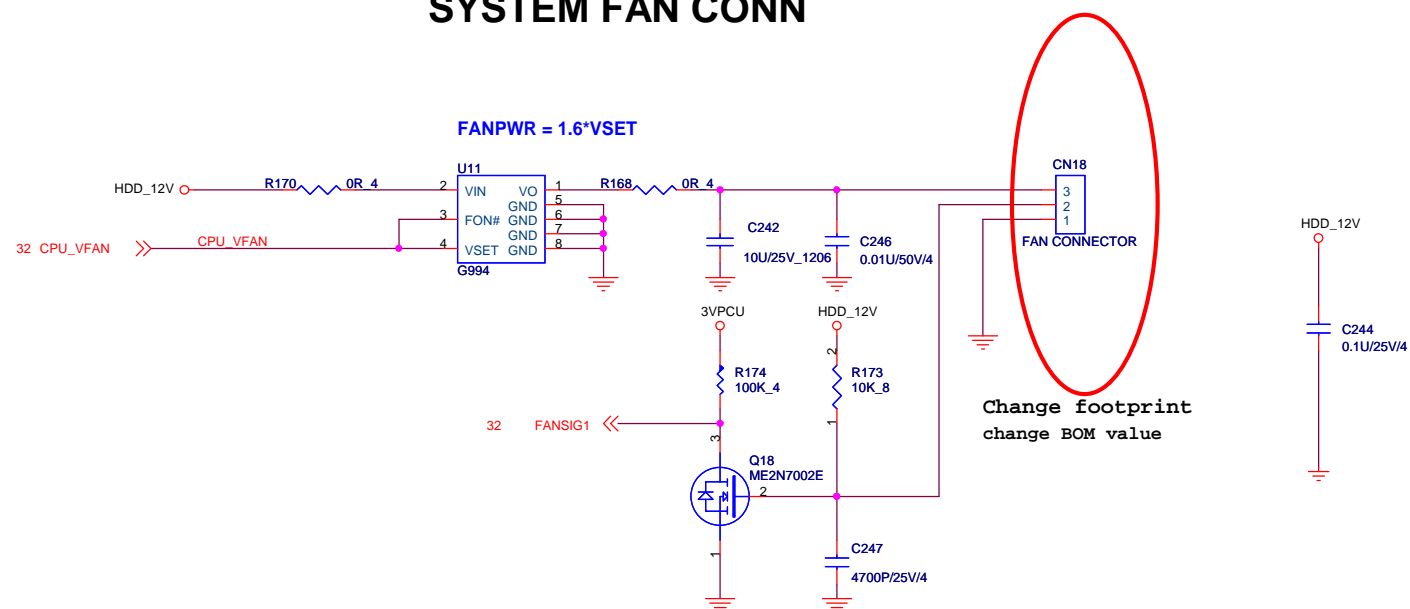
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USB(BLUETOOTH)

L19 change * from Footprint to value

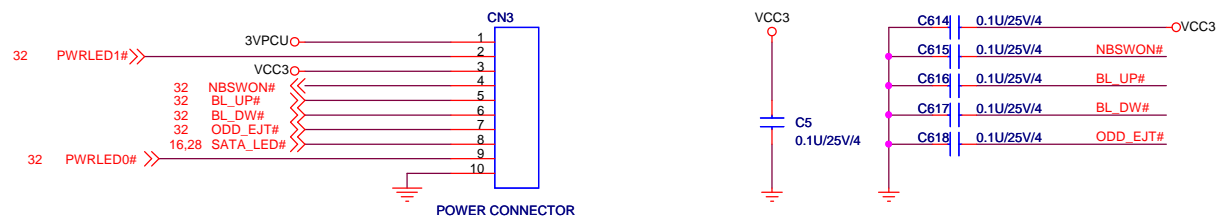


SYSTEM FAN CONN

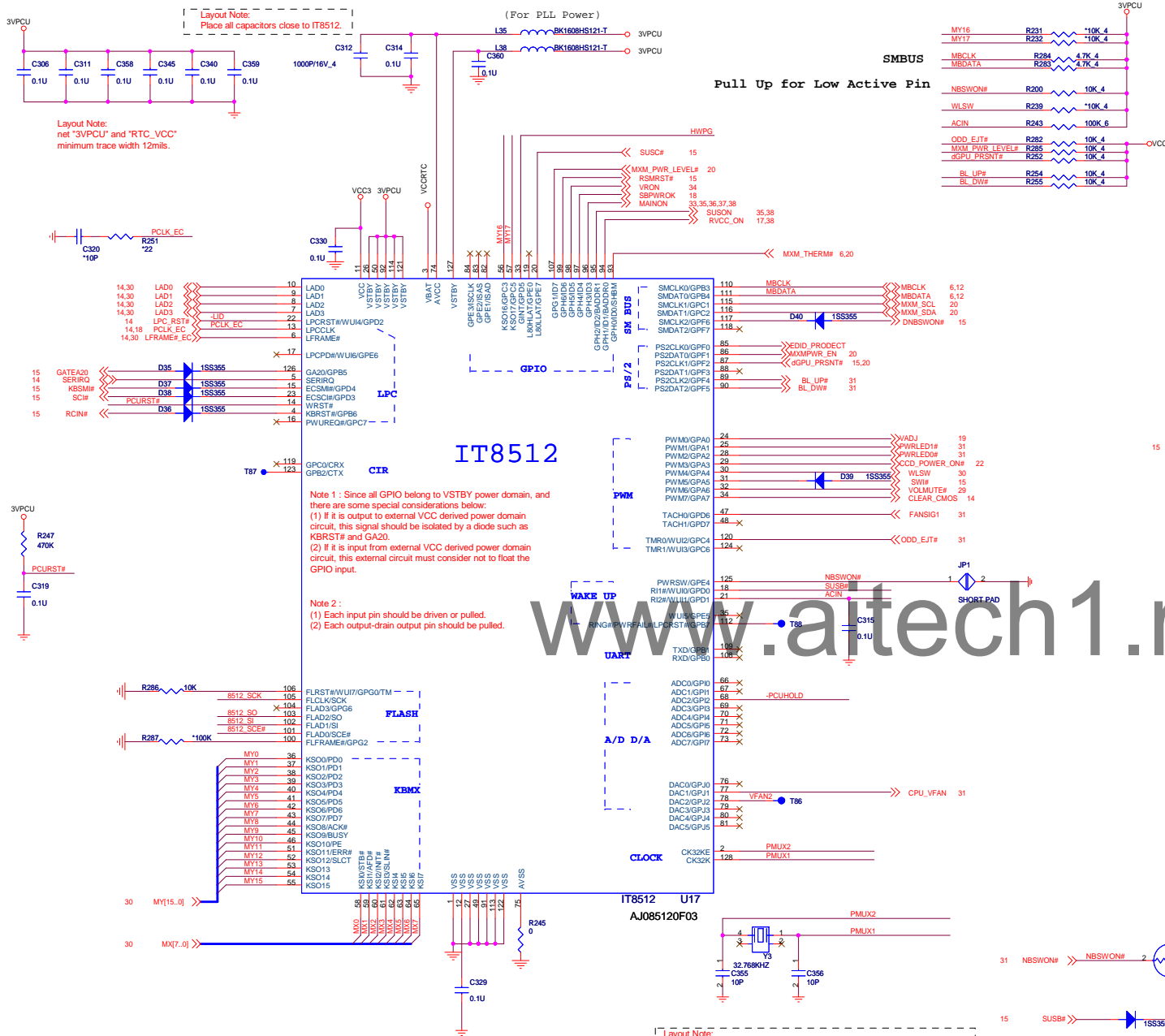


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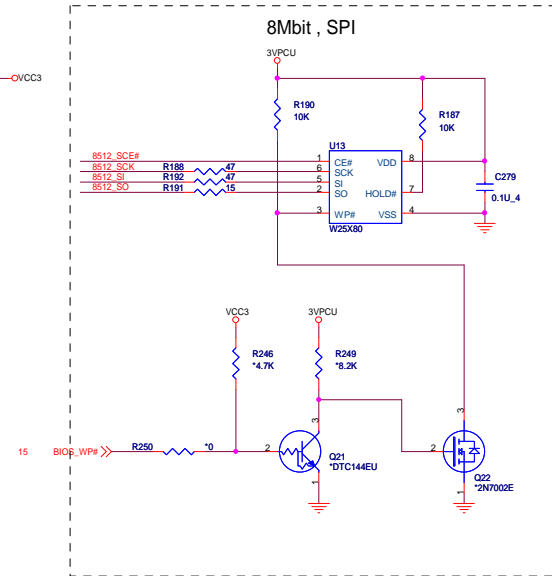
FOR EMI



TO POWER BUTTON & LED LIGHT

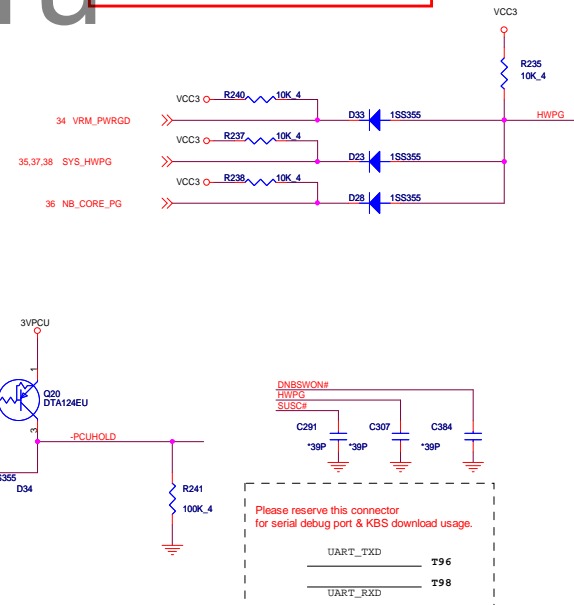


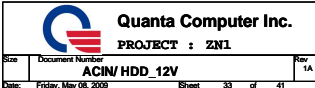
Layout Note:
Place R471, R498, R534 within 500 mils from SPI
Flash. Place R567 within 500mils from R534:
R520 within 500mils from R498 and R570 within
500mils from R471.

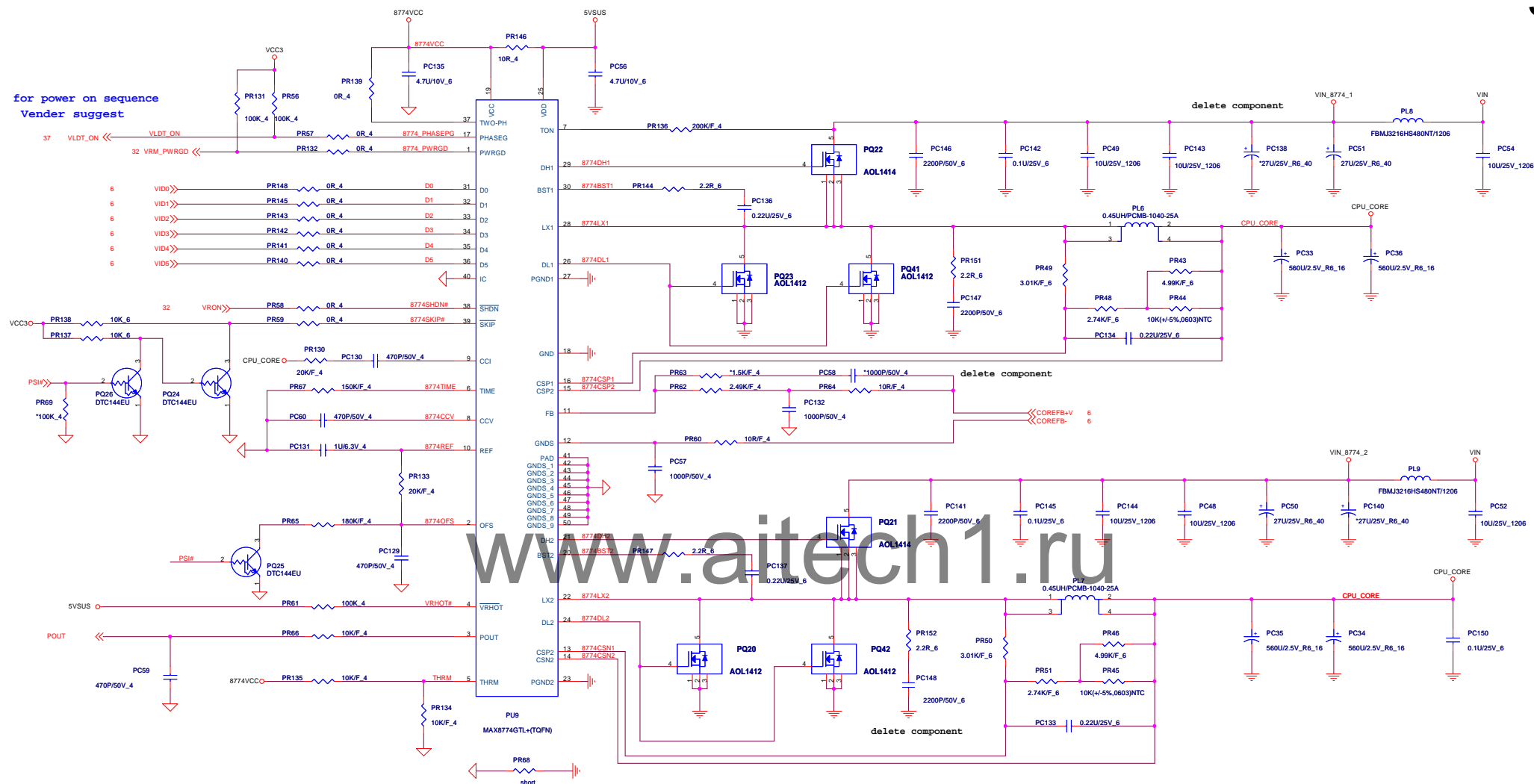


8M Winbond P/N:AKE3GN0N00

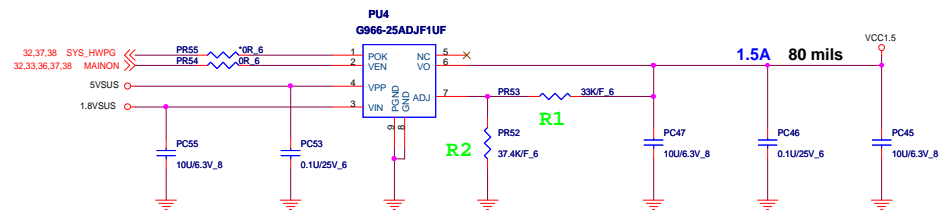
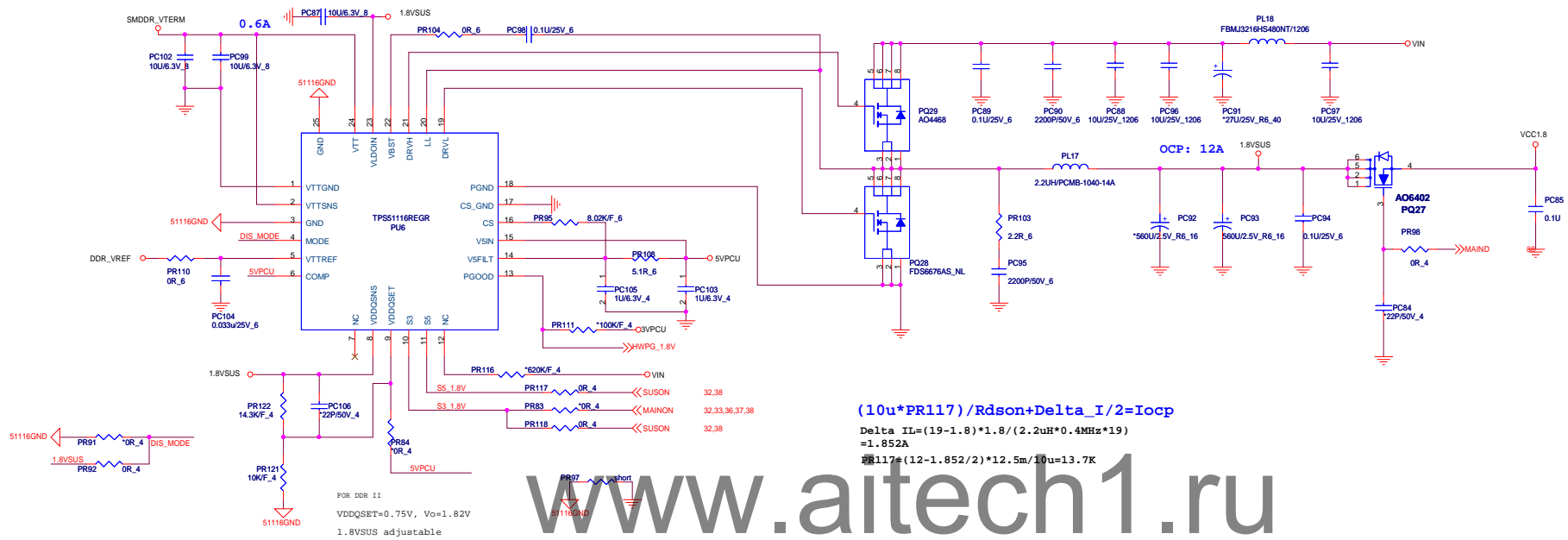
SPI Socket P/N:DG080800031
A stage be use first

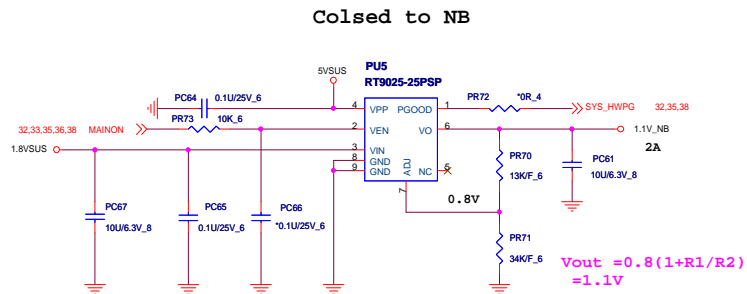
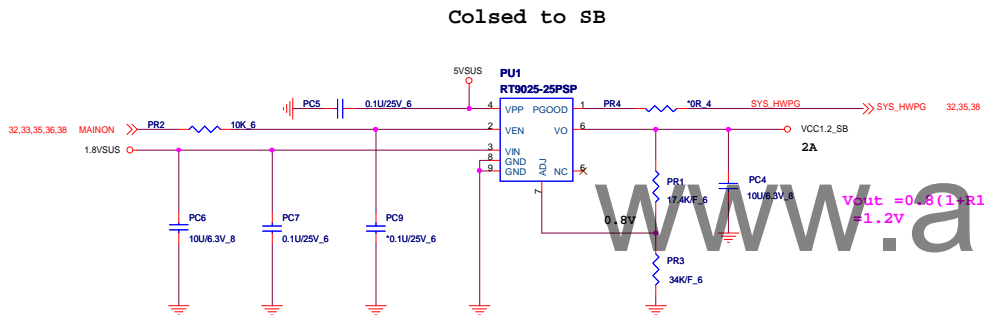
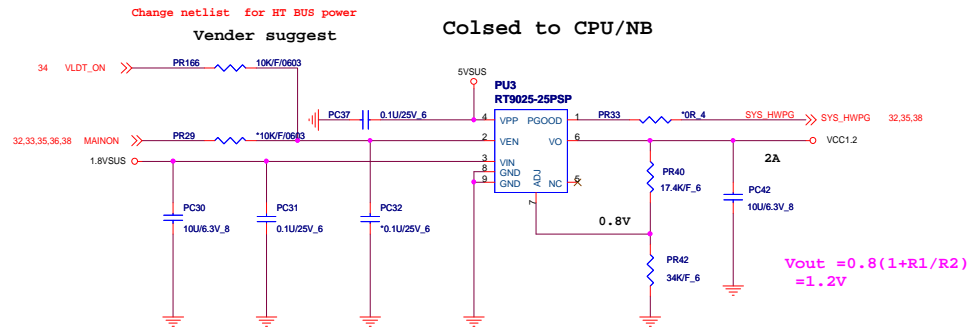


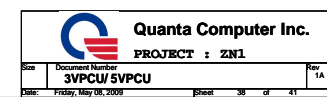


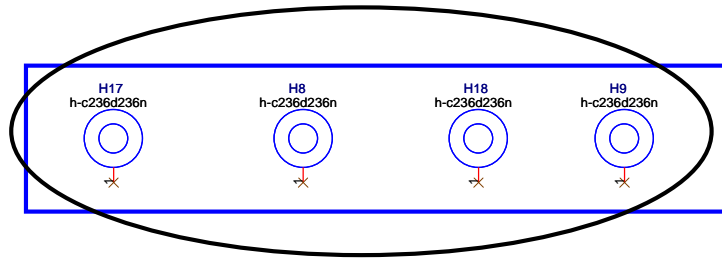


For AMD AM2 CORE

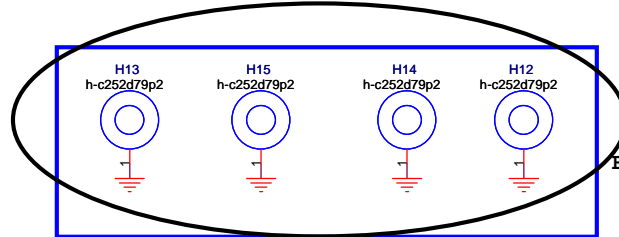




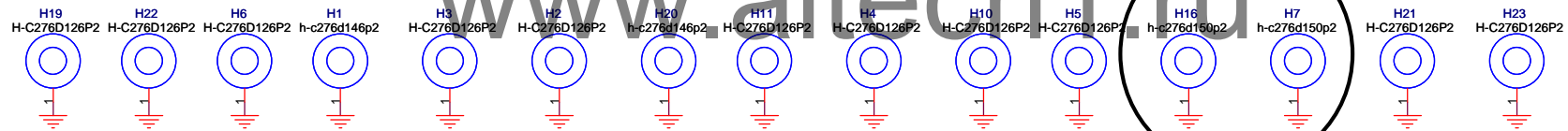




For cpu



For mini card



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PROJECT : ZN1

Size	Document Number	Rev
	SCREW HOLE & EMI	A
Date:	Friday, May 08, 2009	Sheet 39 of 41

DATE

2009

0320

Description

1.change RPl-RP9 to 47 ohm (AMD suggestion)----PAGE 3
2.add R448 10k to VCC3---PAGE 6
3.add R101 300ohm to 1.8VSUS---PAGE 6
4.add R449 10K ohm to VCC3---PAGE12
5.Reserve C612,C613,R441,Y6 to schematic---page14
6.add D59 and R446 10k to VCC3---page14
7.add R455,C621,C622 to schematic for EMI---page14
8.add write EDID rom net to control ---page15
9.delete R403 and R32 --page 15
10.change C91,c95 value to 33p---page 16
11.Add 2 short pin for clear cmos and clear password --page16
12.add R86 10k--page 18
13.delete D4,D5 ,C68 component and add R69 0ohm---page18
14.change netlist to SB control (write_edid _rom)and add R62 2.2k ohm--- page19
15.change Q8 control pin to main pin---page 20
16.change MXM reset from pltrst.---page20
17.add ine out mute function---page23
add component ar35,ar36,ar37,ac38,aq1,aq2,ad2,ad3,q34,q35,r450,r452--page23
18.delete Q26,c475 and change LANVCC net to RVCC3 to control ---page24
19.change C447,C448 to 33p---page 24
20.change CN13 footprint for LED pin change---page 25
21.add ESD protect RV17,RV19,RV13,RV15,RV14,RV16,
RV18,RV20,RV9,RV10,RV11,RV12---PAGE 26
22.Change CN25,CN26 footprint for ME---page26
23.add D18,D19 for XD detect and change net SD_WP#/XD_WP for SD write protect ---page27
24.change LED2 to Green type---page 27
25.change CN8 to rightangle and change odd connect to vertical type for ME---page 28
26.change au6 to OR-gate from AND-gate for pop sound---page 29
27.change fan control net from Vender suggestion.---page 31
28.add c614--618 0.1u for EMI--- page 31
29.add pr165 ,led3 for power line in ---page33
30.change VLDT_ON net for power on sequence--PAGE 34
31.change pr137,pr138 type to BOM---page 34

33.LED RT value need to change

Note

B2B

Page




Quanta Computer Inc.

PROJECT : ZN1

Size	Document Number	Rev
	CHANGE LIST	C
Date:	Friday, May 08, 2009	Sheet 40 of 41

DATE	ZN1 Board file	ZN1 Schematic
11th Mar. 2009	ZN1-0311-17-152.brd	AH1_A_FEB23_01.DSN
31th Mar. 2009	ZN1-0325-1830.brd	ZN1_B_HP_MAR31.DSN

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PROJECT : ZN1

Size

Document Number

Rev

CHANGE LIST

C

Date: Friday, May 08, 2009

Sheet 41 of 41